AUBURN UNIVERSITY
SAMUEL GINN
COLLEGE OF ENGINEERING

Spring 2013

cave³ News

NSF-CAVE3 Electronics Research Center
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INSIDE

Mission Statement

CAVE is dedicated to working with industry in developing and implementing new technologies for the packaging and manufacturing of electronics, with special emphasis on the cost, harsh environment, and reliability requirements of the automotive, aerospace, military, computing, portable and other industries.

Message from Director

In general, automotive systems are often expected to last ten years, hundred thousand miles in service. The use of electronics in automotive applications is widely expected to increase over the near future with the transition to hybrid-electric and fully-electric vehicles. The phase-out of the leaded solders in consumer electronics also means that electronic systems in the newer EV platforms will be largely leadfree. A bigger problem is that the choice for leadfree solder alloy used has not converged and there plethora of new leadfree solder alloys emerging to solve specific performance problems. Further, a major concern from electronics standpoint in light of recent studies at CAVE3 and other research centers, is that commercially viable SnAgCu solders exhibit significant degradation in mechanical properties during operation at high temperatures. Exposure to high temperatures may be largely unavoidable in automotive systems without extensive cooling solutions, which if incorporated may in turn reduce efficiency. There has not been a significant implementation of leadfree solders in aerospace, defense, and high performance applications. There is no consensus on how to address the long-term reliability of mixed-alloy ball-grid array solder joints. The defense systems have high demands in terms of high reliability, mission critical systems, very long service life, operation of extended temperature ranges, and requirement of repairable systems. The DoD acquisition programs are increasingly dependent on commercial off the shelf parts for their electronic modules. Reliability modeling techniques have lagged the emergence of the new leadfree alloys. Nonlinear material constitutive behavior often needed to model the inelastic deformation encountered under prolonged exposure to very-high temperature, very-low temperature, and wide-temperature extremes may not be available for the new emergent alloys. There is often insufficient reliability data to use historic accelerated test databases to develop a warm fuzzy feel for the use of the newer leadfree alloys in high reliability applications. CAVE3 is running long-term aging tests for a wide variety of leadfree parts with multiple leadfree alloys. Some of the data will go towards addressing questions related to reliability degradation from aging.

Energy and water have emerged as two of the bigger engineering grand challenges. Lighting accounts for 17% of the worldwide electricity consumption. Global energy usage is expected to increase. One possible way to address the growing demand for energy is to reduce the energy consumption on lighting. LEDs have seen a tremendous growth in supply and demand. The transition to LEDs is by no-means limited to home or commercial lighting. The lighting revolution has touched televisions to automobiles. LEDs were the dominant form of backlight in LCD televisions and monitors in 2012. There is a need for meaningful accelerated test techniques for LEDs which will help understand failure mechanisms in LEDs prior to new product introduction. CAVE3 is working on development of LED and Luminaire Reliability Models under office benign and outdoor environments.

The Center has acquired extensive capabilities including two large integrating spheres for LED characterization. CAVE3 has also recently acquired a state-of-the art μCT system and Keyence Digital Optical Microscope for non-destructive evaluation of electronics. I want to take this opportunity to welcome new members in the CAVE3 Consortium. New members are Qualcomm, and Siliconware Precision Industries Co., Ltd.

- Pradeep Lall, T. Walter Professor and Director

CAVE³ Consortium Spring Technical Review Meeting

The Center for Advanced Vehicle and Extreme Environment Electronics (CAVE³) will hold its Fall Technical Review and Project Planning Meeting on March 6-7, 2013 in Auburn University Wiggins Hall. All current members of the Consortium are invited to attend. The agenda for this event is available at cave.auburn.edu under CAVE³ Reviews. The following projects will be presented at the meeting:

- Acceleration Factors and Life Prediction Models for on-chip and off-chip Failure Mechanisms
- Advanced Interconnect Systems and 3D-Packaging Architectures in Harsh Environments
- Prognostic Health Monitoring Methodologies for Damage Estimation in Leaded and Lead-Free Solder Alloys
- PHM for Field-Deployed Electronics Subjected to Multiple Thermal Environments
- Leadfree Part Reliability, Crack Propagation and Life Prediction under Extreme Environments
- The Effects of Environmental Exposure on Underfill Behavior and Flip Chip Reliability
- Models for Underfill Stress-Strain and Failure Behavior with Aging Effects
- Insitu Die Stress Measurements in Flip Chip Packaging
- Modeling and Material Characterization for Flip Chip Packaging
- Theoretical and Experimental Investigation on Fretting Corrosion and Thermal Degradation for Hybrid and Electric Vehicles
- Complaint Pin/Press Fit Technology
- Model Simulation and Validation for Vibration-Induced Fretting Corrosion
- Vibration Based Interfaces for Information Transmission
- Microstructural and Mechanical Studies of SAC/Sn-37Pb Mixed Solders
- Aging Behavior of Next Generation Pb-Free Alloys
- Extreme Low Temperature Behavior of Solders
- Composition, Microstructure, and Reliability of Mixed Formulation Solder Joints
- QFP Reliability on Powered and Non-powered Thermal Cycle Environment
- Harsh Environment Substrate Performance
- Module Overmolding for Harsh Environments
- Systems Reliability of Lead Free for Harsh Environment Electronics

A block of rooms has been reserved for Review attendees at the preferred group rate. Room block will expire on September 1, 2012.

Contact Information:
Auburn University Hotel & Conference Center
241 South College Street
Call: (334) 821-8200

SPECIAL EVENTS

CAVE3 is a Technical Co-sponsor for the 2013 IEEE International Conference on Prognostics and Health Management

June 24-27, 2013
National Institute of Standards and Technology, Gaithersburg, MD

The IEEE Reliability Society is proud to sponsor its third annual International Conference on Prognostics and Health Management (IEEE PHM2012). CAVE3 is a technical sponsor for the conference. The 2013 IEEE PHM Conference is bringing together the expertise of relevant technical and management communities to facilitate cross-fertilization in this broad interdisciplinary technical area. This conference provides a sociable, professional environment to network with other practitioners and experts, forge new relationships, and deepen existing ones. The conference will cover a broad range of research and application topics covering the full scope of PHM development, from systems engineering and design to processes, methodology, and barriers to PHM application and implementation. World-renowned speakers will provide presentations, and participate in panel discussions, with a full day of tutorials free to all registrants. Details of the IEEE PHM can be found at www.phmconf.org

Harsh Environment Electronics Symposium Call for Papers

Abstract Deadline: March 15, 2013
Fort Worth Convention Center, Fort Worth, TX
October 14, 2013

The SMTA and CAVE3 at Auburn University are pleased to announce the 2013 AIMS (Automotive, Industrial, Military and Space) Harsh Environment Electronics Symposium. Dr. Pradeep Lall and Dr. John Evans, Conference Chairs and the SMTA International technical committee invite you to submit an abstract to participate in this timely program. The symposium will once again focus on harsh environments with an emphasis on military and space. We are soliciting abstracts that will provide NEW and TIMELY INFORMATION to attendees on the LATEST DEVELOPMENTS in these areas.

Specific subject areas include, but are not limited to:
► Alternative Energy (including, wind, water transportation, battery)
► Components and Component Reliability
► Corrosion
► Extreme Environmental Applications
► Lead-Free Issues for Harsh Environments
► Substrate Surface Finishes for Harsh Environment Applications
► Thermal Management
► Tin Whiskers

Submit abstracts online at www.smta.org/smtai/call_for_papers.cfm

Level of Damage and Remaining Useful Life Assessment in Leadfree Electronics

Field deployed electronics is often subjected to a combination of thermal aging and thermal cycling. The thermal cycle magnitudes may vary over the lifetime of the product. Long-life systems may be re-deployed several times over the use life of the product. Aging has been previously shown to effect the reliability and constitutive behavior of second-level leadfree interconnects. Often the equipment may not have any macro-indicators of damage such as cracks or delamination. The ability to identify impending failures in systems and their sub-components has great potential to mitigate the risks of unanticipated failures and reduce the support costs. The approach developed in this effort is intended to address the need for tools and techniques for prognosticating the prior accrued damage and the remaining useful life of the product prior to redeployment.

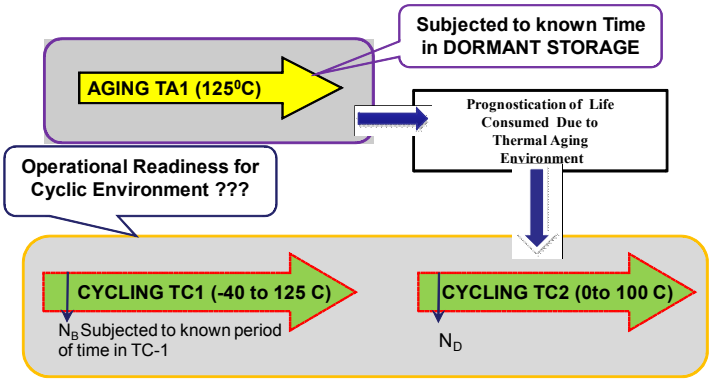


Figure 1: Exposure of Electronics Sequential Stresses of Thermal Aging and Cycling .

Leadfree assemblies with Sn3Ag0.5Cu solder have been subjected to various duration-combinations of thermal aging at 125°C, thermal cycling from -40°C to 125°C and thermal cycling from 0°C to 100°C. The methodology uses leading indicators of failure based on micro-structural evolution of damage to identify accrued damage in electronic systems subjected to sequential stresses of thermal aging and thermal cycling. The presented method for interrogation of the accrued damage for the field deployed electronics, significantly prior to failure, may allow insight into the damage initiation and progression of the deployed system. The expected error with interrogation of system state and assessment of residual life has been quantified.

Classification of Location of Damage in Package-on-Package (PoP) Assemblies using ANN with Feature Vectors

Miniaturization of electronic products has resulted in proliferation of package-on-package (PoP) architectures in portable electronics. In this study, daisy-chained double-stack PoP components have been used for early-identification of drop-shock impact damage. Time-spectral feature vector based damage precursors have been identified and measured under applied shock stimulus. Experimental strain data has been acquired using strain sensors, digital image correlation. Continuity has been measured using high-speed instrumentation for identification of failure in the PoP assemblies. The time-evolution of spectral content of the damage pre-cursors has been studied using joint time frequency analysis (JTFA). The Karhunen-Loéve transform (KLT) has been used for feature reduction and de-correlation of the feature vectors for input to an artificial neural network. The artificial neural net has been trained for failure-mode identification using simulated data-sets created from error-seeded models with specific failure modes. The neural net has then been used to identify and classify the failure modes experimentally observed in tested board assemblies. Supervised learning of multilayer neural net in conjunction with parity has been used to identify the hard-separation boundaries between failure mode clusters in the de-correlated feature space. Pre-failure feature space has been classified for different fault modes in PoP assemblies subjected to drop and shock.

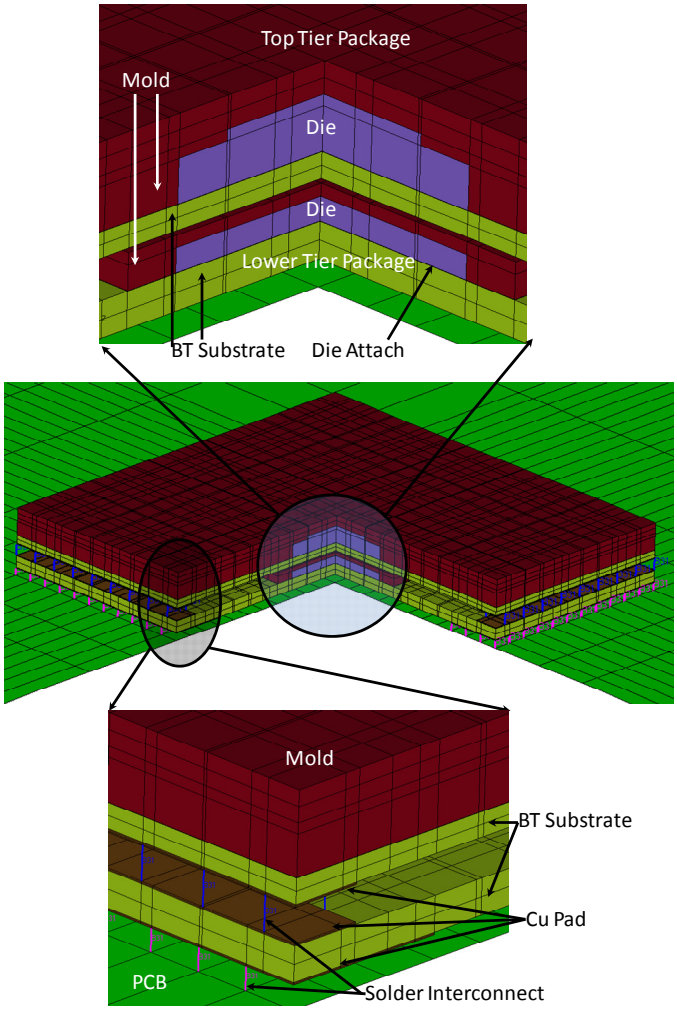
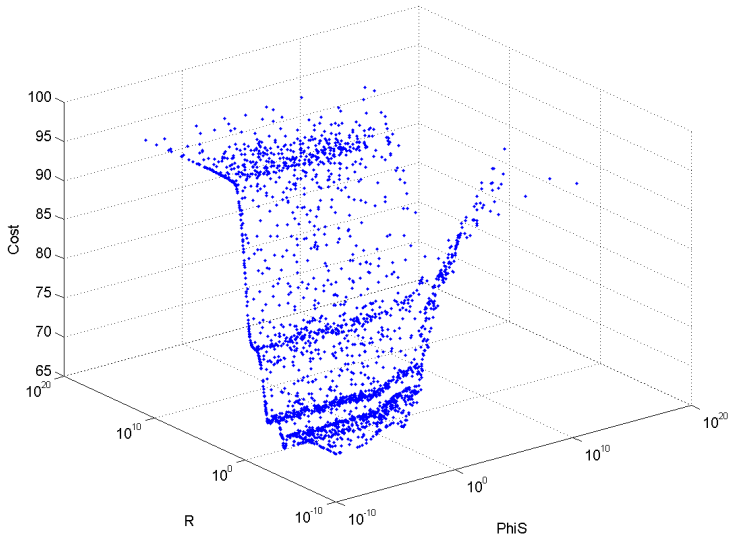


Figure 2: Cross Section of Detailed modeling of PoP module using explicit finite elements on ABAQUS

Research Highlights

Particle Swarm Optimization with Extended Kalman Filter for Prognostication of Accrued Damage in Electronics

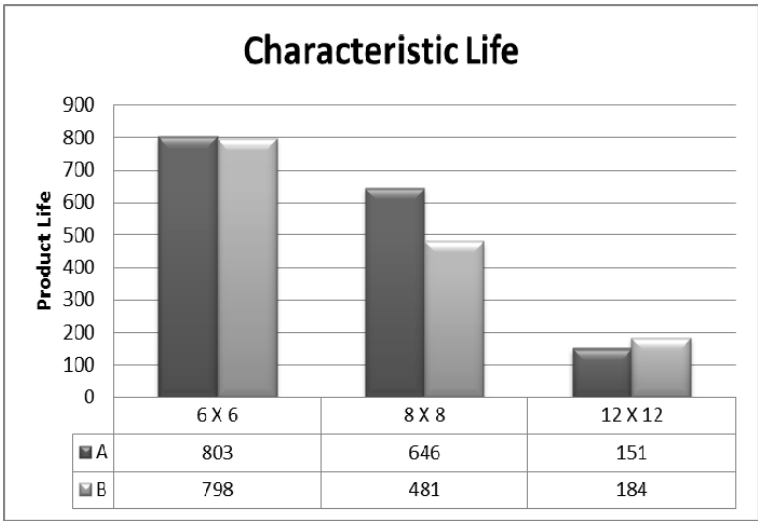
Electronics in harsh environments may be subjected to extended periods of simultaneous high temperature and vibration and stored for prolonged periods of time prior to and during deployment. Damage accrued during the storage and prior usage may reduce the remaining useful life of the electronic system during deployment. Methods for assessment of accrued damage under simultaneous stresses are scarce. In this study, test to failure data has been measured to study the effect of simultaneous thermal and vibration loadings on the reliability of BGA components. Two groups of pristine and isothermally aged components have been tested at both room temperature and 125°C while simultaneously being subjected to vibration loads. The transient response of printed circuit boards under the overlapping stresses has been characterized. Damage accrued under overlapping stresses has been investigated using physics-based leading indicators of damage. The leading indicators are state vectors based on optically measured strains and deformation, resistance spectroscopy and phase sensitive detection. An extended Kalman filter (EKF) is employed to predict remaining useful life (RUL) of the BGA components. A particle swarm optimization (PSO) technique, has been used to robustly demonstrate and quantify the repeatability of the resistance spectroscopy measurements and the accompanying prognostic algorithms.



Search space of the PSO algorithm

DROP RELIABILITY TEST ON DIFFERENT DIMENSIONAL LEAD-FREE WAFER LEVEL CHIP SCALE PACKAGES

In this experiment, a solder ball grid array interconnect has been studied for reliability. The drop performance of different dimensional lead free wafer level chip scale package on laminate assemblies with SAC 305 alloys (3% Ag, 0.5%Cu) were recorded, to determine their reliability based on optimal dimensions of ball grid array and polymer coat package structures.



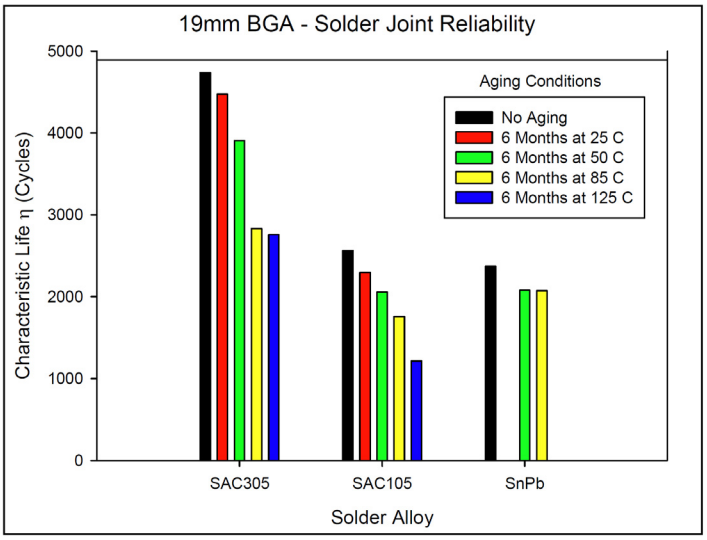
	6 X 6	8 X 8	12 X 12
A	803	646	151
B	798	481	184

Drop Impact Test Characteristic life

The test chips were of 6 X 6, 8 X 8 and 12 X 12 ball grid array packages with perimeter solder balls on a 0.4 mm pitch. The WLCSP assembly was subjected to high impact accelerated life test of 400 drops per board with 1500G, 0.5 millisecond half sine pulse. The test boards were built to withstand JEDEC JESD22-B111 standards of high stress test in drop towers to assess the solder joint performance. Reliability of the test chips were determined from the ability of the solder interconnects to withstand the mechanical stresses induced by the drops. The SAC alloy micro structures of the components were studied in a scanning electron microscope to determine the impact of the intermetallic components on the solder joint reliability. The results showed that the main crack initiation position was at the top side of the solder joints (near the chip side). The results showed that the 6 X 6 ball grid array packages had better reliability and on the 12 X 12 packages the CSP_{n3} had better reliability than the CSP_{n2}.

PREDICTIONS OF LEAD FREE SOLDER JOINT RELIABILITY THAT INCLUDE AGING EFFECTS

It has been demonstrated that isothermal aging leads to large reductions (up to 50%) in several key material properties for lead free solders including stiffness (modulus), yield stress, ultimate strength, and strain to failure. In addition, even more dramatic evolution has been observed in the creep response of aged solders, where up to 10,000X increases have been observed in the steady state (secondary) creep strain rate (creep compliance). Such degradations in the stiffness, strength, and creep compliance of the solder material are expected to be universally detrimental to reliability of solder joints in electronic assemblies. Traditional finite element based predictions for solder joint reliability during thermal cycling accelerated life testing are based on solder constitutive equations (e.g. Anand viscoplastic model) and failure models (e.g. energy dissipation per cycle models) that do not evolve with material aging. Thus, there will be significant errors in the calculations with lead free SAC alloys that illustrate dramatic aging phenomena.

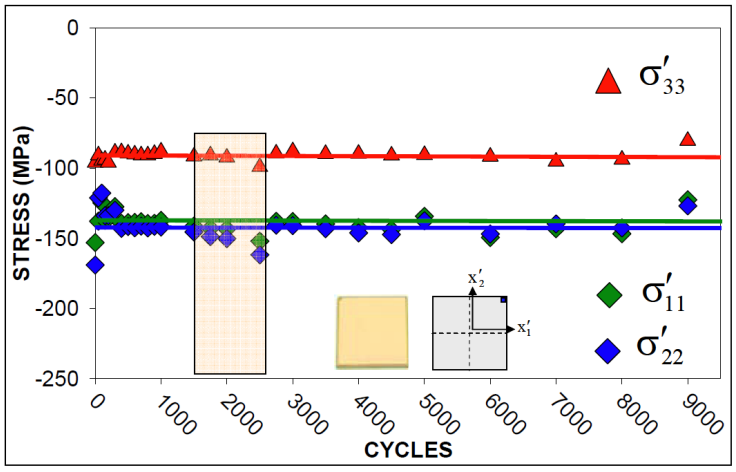


Effect of Aging on Characteristic Life of 19mm BGA

In our current research, we are developing new reliability prediction procedures that utilize constitutive relations and failure criteria that incorporate aging effects, and then validating the new approaches through correlation with thermal cycling accelerated life testing experimental data. In this paper, we report on the first step of that development, namely the establishment of a revised set of Anand viscoplastic stress-strain relations for solder that include material parameters that evolve with the thermal history of the solder material. The effects of aging on the nine Anand model parameters have been examined by performing stress-strain tests on SAC305 samples that were aged for various durations (0-6 months) at a temperature of 100 C. For each aging time, stress-strain data were measured at three strain rates (0.001, 0.0001, and 0.00001 1/sec) and five temperatures (25, 50, 75, 100, and 125 C). Using the measured stress-strain data, the Anand model material parameters have been determined for various aging conditions. Mathematical expressions were then developed to model the evolution of the Anand model parameter with aging time. Our results show that 2 of the 9 constants remain essentially constant during aging, while the other 6 show large changes (30-70%) with up to 6 months of aging at 100 C. Preliminary finite element simulations have also shown that the use of the modified Anand model leads to a strong dependence of the calculated plastic work dissipated per cycle on the aging conditions prior to thermal cycling.

DIE STRESSES IN MICROPROCESSOR PACKAGING IN THERMAL AND POWER CYCLING

The increasingly complex packaging used in modern workstations and servers transmits a complicated set of mechanical loads to the microprocessor. Increasing die size, high CTE ceramic substrates, lead free solder joints, and ever increasing power requirements have led to increased die stress levels in packaged microprocessor die. Such stresses can degrade silicon device performance, as well as damage the copper/low-k interconnect layers, and in extreme cases, mechanical failure of the die may occur. In previous work of the authors, on-chip piezoresistive stress sensors have been utilized to quantify stress levels induced by microprocessor packaging processes such as flip chip solder joint reflow, underfill cure, and lid attachment. Good correlation has been obtained between the test chip measurements and finite element simulations of the flip chip ceramic ball grid array (FC-CBGA) component assembly process.



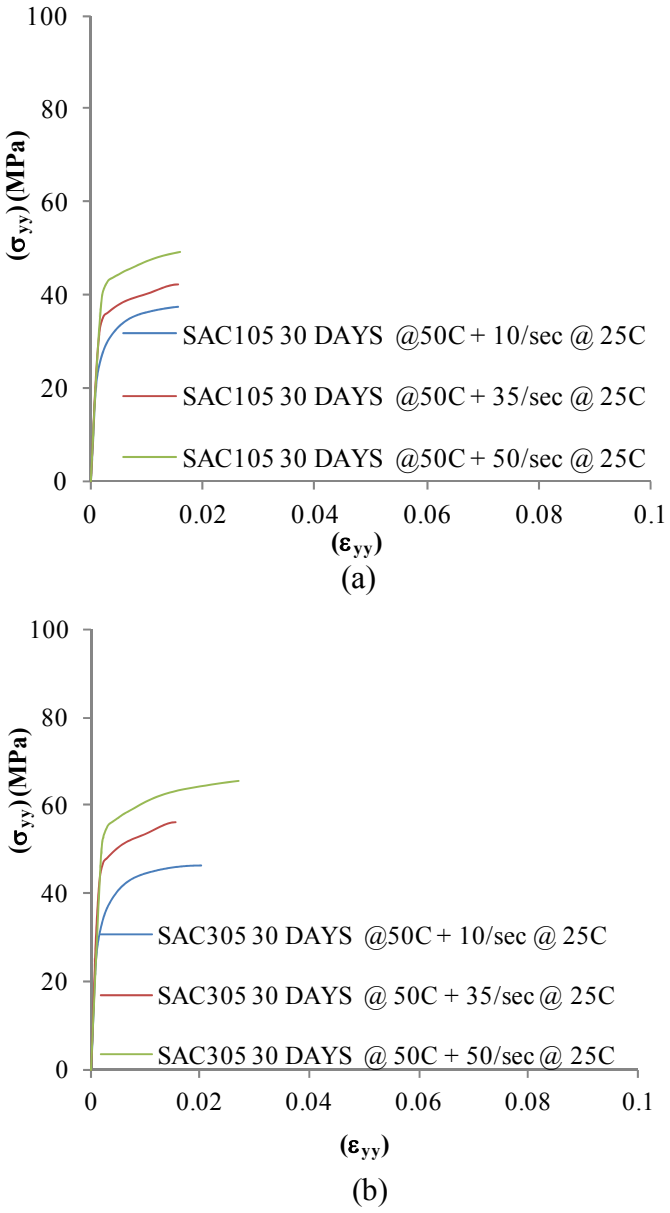
Variation of the Average Stresses at the Die Corner with Thermal Cycling

In the current work, we have extended our past studies on the FC-CBGA microprocessor packaging configuration to investigate in-situ die stress variation during thermal and power cycling. The utilized (111) silicon sensor rosettes were able to measure the complete three-dimensional stress state (all 6 stress components) at each sensor site being monitored by the data acquisition hardware. The test chips had dimensions of 20 x 20 mm, and 3600 lead free solder interconnects (full area array) were used to connect the chips to high CTE ceramic chip carriers. A unique package carrier was developed to allow measurement of the die stresses in the FC-CBGA components under thermal and power cycling loads without inducing any additional mechanical loadings. Initial experiments consisted of measuring the die stress levels while the components were subjected to a slow (quasi-static) temperature changes from 0 to 100 C. In later testing, long term thermal cycling of selected parts was performed from 0 to 100 C (40 minute cycle, 10 minute ramps and dwells). After various durations of cycling, the sensor resistances at critical locations on the die device surface (e.g. die center and die corners) were recorded. From the resistance data, the stresses at each site were calculated and plotted versus time. Finally, thermal and power cycling of selected parts was performed, and in-situ measurements of the transient die stress variations were performed. Power cycling was implemented by exciting the on-chip heaters on the test

HIGH STRAIN-RATE MECHANICAL PROPERTIES OF SAC105 AND SAC305 ALLOYS

Electronics may experience high strain rates when subjected to high g-loads of shock and vibration. Material and damage behavior of electronic materials at high strain rates typical of shock and vibration is scarce. Previously studies have shown that second-level interconnects have a high propensity for failure under shock and

vibration loads in fine pitch electronics. Exposure to shock and vibration is common in a variety of consumer environments such as automotive and portable electronics. The low strain-rate properties of commonly used SnAgCu solders, including Sn1Ag0.5Cu and Sn3Ag0.5Cu, have been found to evolve with time after prolonged exposure to high temperatures.

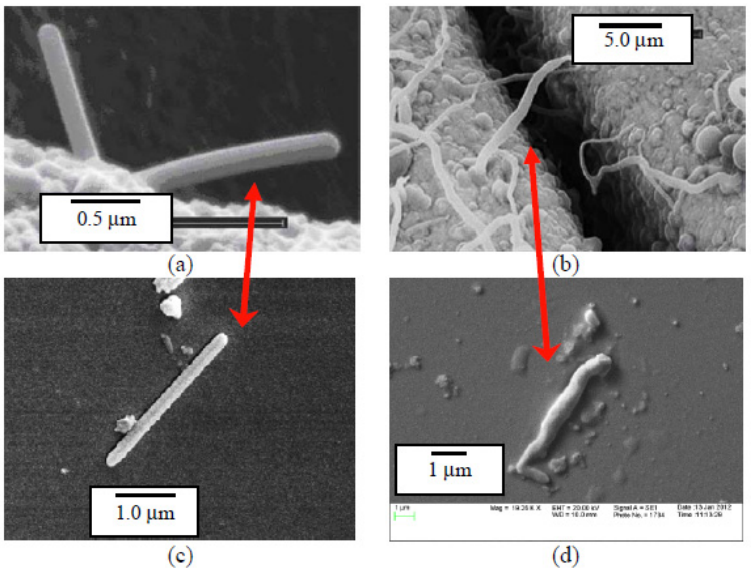


Stress vs. Strain for 30-days elevated temperature (50C) aged SAC105 and SAC305 alloys respectively

High strain rate properties of leadfree solder alloys in the strain-rate range of 1-100 sec^{-1} are scarce. Previous attempts at characterizing the high strain rates properties have focused on the use of the Split Hopkinson Pressure Bar (SHPB), which enables measurements of strain rates in the neighborhood of 1000 per sec. In this paper, a new test-technique developed by the authors has been presented for measurement of material constitutive behavior. The instrument enables attaining strain rates in the neighborhood of 1 to 100 per sec. Tests are conducted at strain rates 10, 35 and 50 per sec. High speed cameras operating at 75,000 fps have been used in conjunction with digital image correlation for the measurement of full-field strain during the test. Constancy of cross-head velocity has been demonstrated during the test from the unloaded state to the specimen failure. Solder alloy constitutive behavior has been measured for SAC105, SAC305 solders. Non-linear Ramberg-Osgood model has been used to fit the material data. The Ramberg-Osgood model available in Abaqus has been used for tensile test simulation and to correlate with DIC based experimental strain data.

INFLUENCE OF SURFACE OXIDES ON WHISKERING

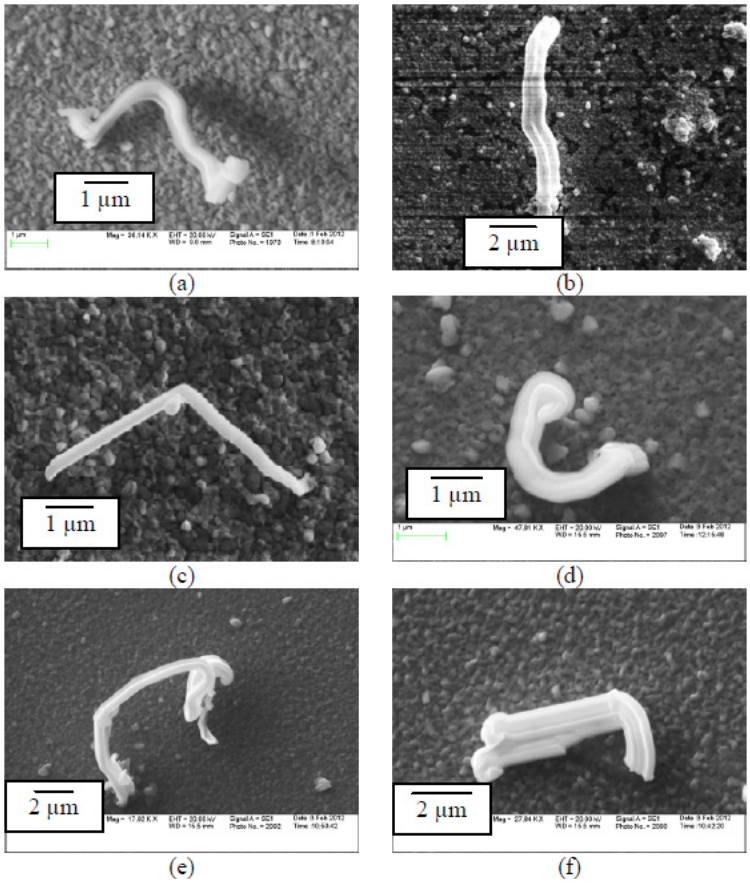
Some mechanistic models of tin (Sn) whisker growth presume that surface oxidation plays an important role in whisker formation. The notion is that Sn whiskers grow through weak spots in the Sn oxide, which is cracked during whisker growth and propagation. It is often implied that a surface oxide is necessary for whisker growth. However, the premise of a surface oxide requirement for whiskering is clearly questionable. Not only have there been anecdotal reports of Au whiskers, but studies by Moon, Handwerker, et al. [31] and our laboratory show that Sn whiskers can grow from atomically clean surfaces and/or surfaces having extremely low amounts of oxygen. This work reports a definitive test of the surface oxidation hypothesis by attempting to grow whiskers from surfaces having no native oxide (Au). The results show that high aspect ratio Au whiskers can be grown within a few weeks from intrinsically (compressively) stressed thin films of sputtered Au on silicon.



Au whisker morphological comparison. (a)-(b) Au Whiskers observed by by A. Teverovsky [30]; (c)-(d) Au whiskers observed at CAVE3

WHISKER PREVENTION USING HARD METAL CAP LAYERS

Application of conformal coatings has shown promise as a practical scheme for preventing whisker growth in electronic assemblies. Coatings have been proposed utilizing elastomeric, ceramic, and metallic materials. The ability to prevent whiskers is particularly important in assemblies containing Pb-free materials and finishes. Further, many otherwise desirable COTS (commercial off the shelf) electronic components and assemblies are available only with Pb-free tin as the termination finish or Pb-free SAC solder balls under BGAs. In this work we have investigated a variety of proposed whisker-impenetrable hard metal caps through use of Auger electron spectroscopy (AES) and Rutherford backscattering spectroscopy (RBS) and discuss plausible reasons why only certain metals are effective in blocking Sn whiskers.

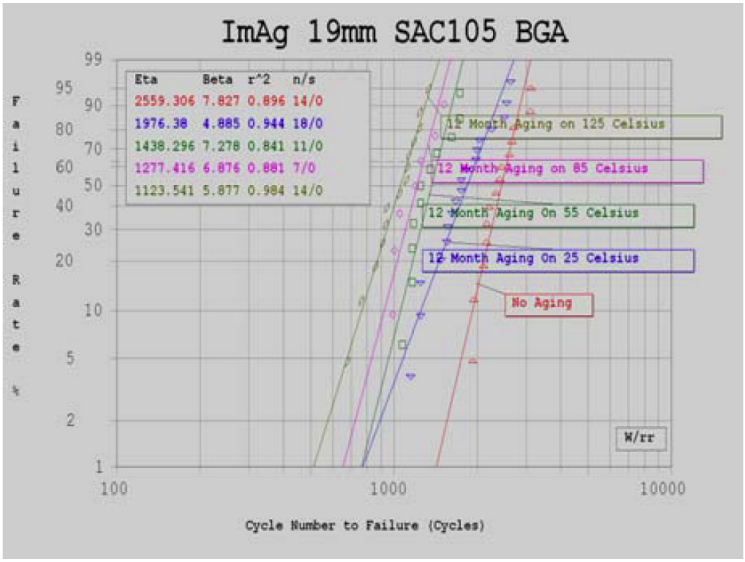


SEM Images of representative whiskers penetrating (a) 875 Å Au Film (b) 1750 Å Au Film (c) 875 Å Au Film (d) 250 Å Cr Film (e) 700 Å Cr Film and (f) 700 Å Cr film.

On compressively stressed Sn films, Ni and Pt metal cap films successfully blocked all Sn whiskers over long incubation times, with the exception of a lone whisker which penetrated the thinnest (350Å) Ni film. In contrast, all Au films were penetrated after ~ 1 month and all Cr films were penetrated after ~ 2 months of incubation. Penetrating whiskers which carry up a fractured piece of the metal cap layer during the puncture process helps to explain why only certain metal caps block whiskers. Cap metals with high shear moduli are likely to block whiskers since cap penetration appears to be a metal punching process. Shear modulus values for the pure elemental cap films approximately follows the trend for whisker prevention metals, with the exception of Cr. The true situation is more complex than this simple mechanical picture, owing to the formation of intermetallic compounds in the cap films and/or diffusion of Sn into the cap. After ~3 months of incubation, diffusion between the cap/Sn films was found in all Au and Cr samples except the thicker, 3000 Å Au film. In addition, a significant amount of incorporated O was observed in Cr cap films due to the low and negative Gibbs free energy of formation of Cr oxides. Only the thinnest, 325 Å Pt and 350 Å Ni films experienced any cap/Sn film mixing at 3 months of incubation. Sn mixing in all Ni films was detected after an extended incubation period of ~16 months. Accurate measurements of shear moduli for the case of intermetallic compounds and further studies of film diffusion at room temperature are necessary for additional insight on why only a few cap metals prevent whisker penetration.

ISOTHERMAL AGING EFFECTS ON HARSH ENVIRONMENT PERFORMANCE OF LEAD-FREE SOLDER JOINTS

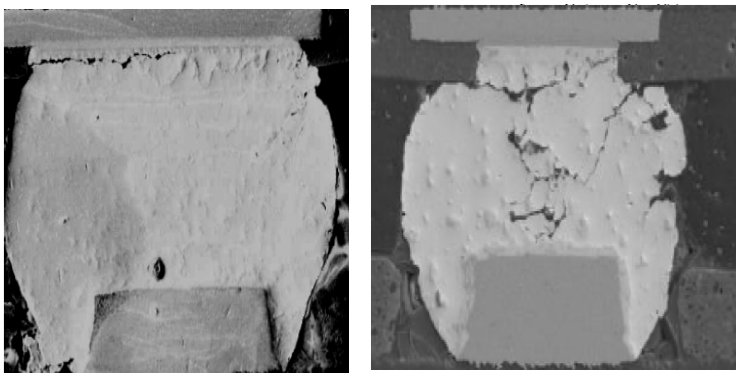
Electronics assemblies containing solder joints are often exposed to elevated temperatures for prolonged periods of time. The time-at-temperature stress impacts the overall package reliability of the assembled circuitry due to evolving materials, microstructural, and mechanical properties. It is especially important to understand the impact of isothermal aging on the long term behavior of lead (Pb)-free solder joints which operate in harsh environments.



Weibull plots vs. thermal cycle for 12 month isothermally aged 19mm BGA samples

In this study, we have explored the effects of elevated temperature isothermal aging on the reliability of Sn-Ag-Cu (SAC) assemblies on board level packages. As the isothermal aging temperature increases, the Weibull characteristic lifetime for SAC 105 and 305

solder joints is drastically reduced compared to Sn-37Pb.In parallel mechanical studies on bulk solder specimens, the creep rate for SAC105, 305 rapidly increases with aging. A full test matrix with varying aging temperatures and solder alloys was considered. Package sizes ranged from 19mm body size, 0.8mm pitch ball grid arrays (BGAs) to 5mm body size, 0.4mm pitch μBGAs. The test structures were built on three different board finishes (ImSn, ImAg and SnPb). Storage condition temperatures were 25°C, 55°C, 85°C and 125°C with aging over time periods of 0, 12 months. Subsequently, the specimens were thermally cycled from -40°C to 125°C with 15 min dwell times at the high temperature. It was found that the thermal performance of lead-free fine-pitch packages significantly degrades up to 55-60% after aging at elevated temperature.



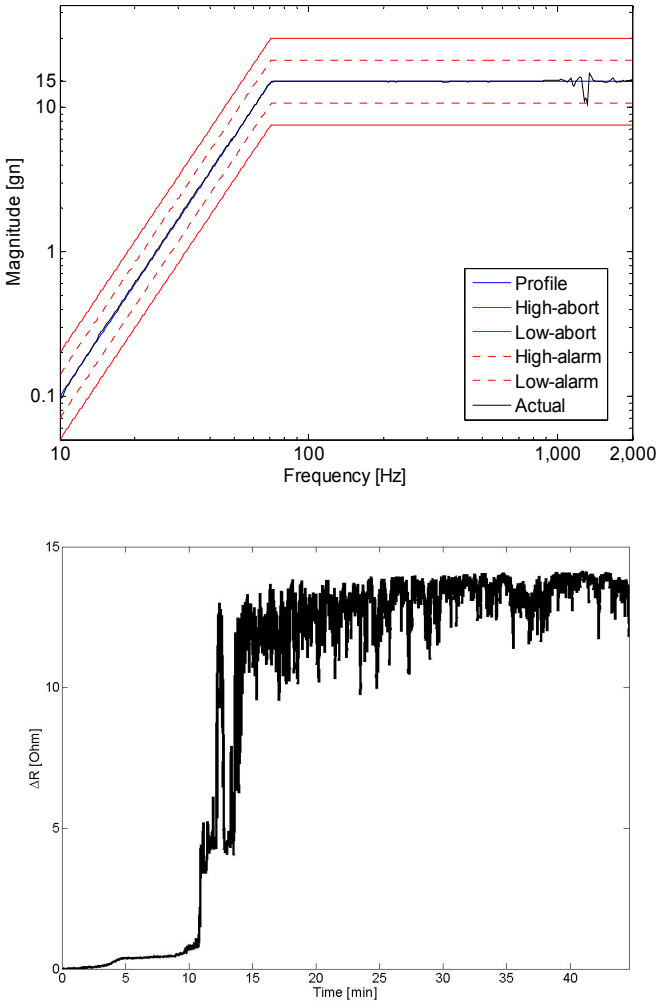
(a) (b)

Failure modes for (a) Unaged 19mm BGAs in thermal cycling (b) 19mm BGAs aged at 85C for 12-months in thermal cycling

Significant cycle lifetime degradation was observed for both SAC105 and SAC305 in 19mm, 15mm, 10mm, 5mm PBGA packages, CSP, and QFN. For the case of 19mm SAC105, there is a 55% reduction in characteristic lifetime at 125$_o$C aging and a 32% reduction at 85$_o$C. The 19mm SAC305 package lifetime decreased by 50% at 125$_o$C. For smaller ball sizes in 10mm and 5mm BGAs, 55$_o$C and 85$_o$C aging caused measurable losses in the lifetime of both SAC105 and SAC305. The 5mm SAC105 decreased by 50% during 125$_o$C/12 months. Smaller solder balls were more sensitive to aging reductions in lifetime. Failure analysis showed significant bulk Ag_3Sn coarsening and intermetallic Cu_6Sn_5 growth at the solder joint interfaces. After 85$_o$C and 125$_o$C aging, the cracks appeared at the lower corners at the board side interface and propagated along the Cu_6Sn_5. The reduced Weibull lifetimes occur coincidently with increasing Cu_6Sn_5 layer growth at board and package sides of the solder joint.

LEADING INDICATORS FOR FAILURE PROGNOSIS OF ELECTRICAL CONNECTORS SUBJECTED TO RANDOM VIBRATION

In this study, leading indicators of failure have been developed to monitor the progression of fretting corrosion in electrical connectors and prognosticate remaining useful life. Connectors subjected to harsh environments may experience vibration resulting in fretting corrosion and degradation in contact resistance over time. Tin coated, rectangular-pin and socket electrical connectors have been studied. Connectors are extensively used in automotive systems in conjunction with wire harnesses. Electronics may be fullfilling many vehicle performance critical functions including: collision avoidance, lane departure warning, supplemental restraint, and driver distraction detection.



(a) Random Vibration Profile at 10gs (b) Connector Resistance from Resistance Spectrocopy

Connector degradation may cause electrical failure during or prior to vehicle operation. In this effort, a random vibration test profile has been used to stimulate the contact resistance degradation due to connector fretting corrosion. The contact resistance has been measured in situ using the resistance spectroscopy method in conjunction with phase sensitive detection. It has been shown that precise resistance spectroscopy and phase measurements can provide a leading indicator of failure significantly prior to the traditional definition of failure.

Announcements

Kewal Patel's poster receives an Honorable Mention Award in the Graduate Engineering Research Showcase

The Graduate Engineering Research Showcase (GERS) is held every year to give graduate students an opportunity to present their research to others and to gain experience in presentation skills. The 2012 Fall GERS was held on September 13, 2012 with over 170 participants from all engineering fields. Students were given an opportunity to observe the research of their peers while also presenting their own findings. Each student was assigned two judges who scored the students based on the quality of the poster and the presentation skills of the presenter. Kewal Patel, a student working under CAVE3, won an Honorable Mention Award for the showcase with his poster titled *Modeling and Reliability Characterization of Area-Array Electronics Subjected to High-G Mechanical Shock up to 50,000G*. The Honorable Mention ranks him among the Top 8 out of all the participants.

Lall and Suhling Ranked in Top Academic Publications Search

Pradeep Lall, Thomas Walter Professor and Director CAVE3, and Jeff Suhling, Quina Professor and Department Chair have been ranked in the top 100 out of a million engineering researchers and publications by Microsoft Academic Search. Lall's research interests include electronic packaging with emphasis on design, modeling, reliability, prognostics, and predictive techniques. Suhling's research interests include electronic packaging, silicon sensors, mechanics of solders, paper and other wood-based materials. Microsoft Academic Search is a free service intended to search for academic content, researchers, institutions, and activities.

Lall Appointed to IEEE Reliability Society Fellows Committee

Pradeep Lall has been appointed to serve on the IEEE Reliability Society Fellows Committee. Lall was elected Fellow of the IEEE in 2012. The Reliability Society provides a professional home for Specialty Engineering communities or disciplines covering not only Reliability Engineering, but also Integrity, System Safety, Prognostics and Health Management (PHM) Testability, System Security, Human System Interface (HSI), Human Factors (HF), Maintainability, and Supportability Engineering disciplines, Software Engineering with a focus on trust, system security, privacy and cybersecurity.

Lall Serves as Steering Committee Chair of ASME International Mechanical Engineering Congress

Pradeep Lall serves as steering committee chair of the American Society of Mechanical Engineers (ASME) Congress 2012. The ASME International Mechanical Engineering Congress and Exposition, held Nov. 9-15 in Houston, Texas, is an premier global conference that features research updates, technical challenges and breakthrough innovations that are shaping the future of engineering.

Lall cuts the ribbon to open the ASME Congress November 11, 2012 in Houston, TX. Pictured from left-to-right: Tom Loughlin (ASME Executive Director), Mina Pelegri (IMECE Technical Program Chair), Aaron Knobloch (IMECE 2012 General Chair), Pradeep Lall (IMECE 2012 CSC Chair), Madiha Kotb (ASME President Elect Nominee), Mark Goldsmith (ASME President), Victoria Rockwell (ASME Past President).

Lall presides over Keynote Session at the ASME Congress 2012

The congress assembles engineers, scientists and technologists of all disciplines to explore solutions to global challenges for the advancement of engineering excellence worldwide. This year's conference included more than 3600 slide and poster presentations, as well as a

record number of more than 640 technical sessions. Congress kicked off with the keynote presentation on by Thomas L. Friedman from The New York Times on Energy Diversity, which reflects the Congress's overall theme: Energy. Prominent Keynote speakers included LTC Nathan Wiedenman from DARPA on the development of complex systems through rapidly reconfigurable manufacturing methods, Rustom K. Mody of Baker Hughes Inc. who spoke about the function of fundamental research as a crucial component to new technologies in the Energy sector, Michael Coats Director of the Johnson Space Center.

Lall Receives Service Award from the BTKD

Pradeep Lall received the Service Award for his role as the Chair of CSC for the ASME Congress 2012. The award was given by Prof. H.S. Tzou, Chair of the Board for Technical Knowledge Dissemination at the BTKD meeting in Houston, TX.

Lall received service award from H.S. Tzou

Lall Appointed Representative on IEEE-USA Government Relations Council for Research and Development Policy

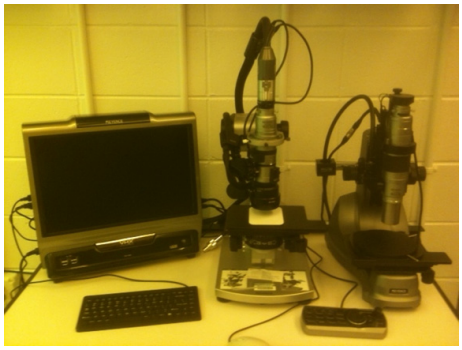
Pradeep Lall has been appointed as the IEEE Reliability Society Representative on the IEEE-USA Government Relations Council for Research and Development Policy. The purpose of IEEE-USA's government relations committees (herein Committees), as specified in their charters, is to inform and influence policymakers about policy issues with significant technological content in which IEEE-USA has expertise. Products and activities of the committees include Policy or Position Statements; testimony before executive, legislative or regulatory bodies; meetings with staff members and/or legislators; letters to newspapers or other publications; technology policy symposia; and other activities. The committees perform their work primarily through the efforts of IEEE-USA volunteers, who provide the technical and policy expertise either through their individual abilities or through their liaison with technical societies and regions (through liaison representatives and Technical Information Statements).

CAVE3 Acquires μCT System

The CAVE3 Electronics Research Center has acquired a Micro-CT system for non-destructive evaluation of electronic packages and assemblies. In addition, volume graphics reconstruction modules has also been procured. The system is capable of 3D rendering of internal structure of semiconductor packaging, in addition to detection of failure modes such as wire bond lifts, solder joint cracks, voids, printed circuit board delamination.

Images Courtesy of Yxlon

CAVE3 Acquires Keyence Digital Optical Microscope



The CAVE3 Electronics Research Center has acquired a Keyence Digital Optical Microscope system for non-destructive evaluation of electronic packages and assemblies. The microscope is capable of 5000X magnification.

Selected Recent Publications

1. Lall, P., Harsha, M., Goebel, K., Level of Damage and Remaining Useful Life Assessment in Leadfree Electronics Subjected to Multiple Thermo-mechanical Environments, IEEE PHM Conference, Denver, CO, June 18-21, 2012
2. Lall, P., Gupta, P., Goebel, K., "Classification of Location of Damage in Package-on-Package (PoP) Assemblies using ANN with Feature Vectors for Progression of Accrued Damage", IEEE PHM Conference, Denver, CO, June 18-21, 2012
3. Lall, P., Lowe, R., Goebel, K., "Particle Swarm Optimization with Extended Kalman Filter for Prognostication of Accrued Damage in Electronics Under Temperature and Vibration", IEEE PHM Conference, Denver, CO, June 18-21, 2012
4. Lall, P., Shantaram, S., Locker, D., "Reliability Modeling of Electronic Systems Subjected to High Strain Rates", IEEE EuroSimE, Cascias, Portugal, 2012
5. Lall, P., Harsha, M., Goebel, K., Jones, J., "Interrogation of Thermo-Mechanical Damage in Field-Deployed Electronics", EuroSimE, Cascias, Portugal, 2012
6. Lall, P., Shantaram, S., Kulkarni, K., Limaye, G., "High Strain-Rate Mechanical Properties of SnAgCu Lead-Free Alloys", Electronic Components and Technology Conference, ECTC, 61st, pp.684-700, 2012.
7. Jackson, R., Crandall, E., Bozack, M., "An Analysis of Scale Dependent and Quantum Effects on Electrical Contact Resistance between Rough Surfaces", Holm, 2012
8. Ghaednia, H., Rostami, A., Jackson, R., "The Influence of Thermal Expansion and Plastic Deformation on a Thermo-electro Mechanical Spherical Asperity Contact", Holm, 2012
9. Crandall, E., Flowers, G., Lall, P., Bozack, M., "Whisker Prevention Using Hard Cap Layers", Holm, 2012
10. Crandall, E., Flowers, G., Lall, P., Snipes, E., Bozack, M., "The Influence of Surface Oxides on Whiskering", Holm, 2012
11. Lall, P., Patel, K., Lowe, R., Strickland, M., Blanche, J., Geist, D., Montgomery, R., Modeling and Reliability Characterization of Area-Array Electronics Subjected to High-G Mechanical Shock Up to 50,000G, Proceedings of the 62nd ECTC, pp. 1194 – 1204, 2012.
12. Lall, P., Harsha, M., Suhling, J., Goebel, K., Sustained Damage and Remaining Useful Life Assessment in Leadfree Electronics Subjected to Sequential Multiple Thermal Environments, Proceedings of the 62nd ECTC, pp.1695-1708, 2012.
13. Lall, P., Lowe, R., Goebel, K., Prognostication of Accrued Damage in Board Assemblies Under Thermal and Mechanical Stresses, Proceedings of the 62nd ECTC, pp.1475 - 1487 , 2012.
14. Lall, P., Shantaram, S., Suhling, J., Locker, D., Effect of High Strain-Rate on Mechanical Properties of SAC105 and SAC305 Leadfree Alloys, Proceedings of the 62nd ECTC, pp. 1312 - 1326, 2012
15. Roberts, J., Motalab, M., Hussain, S., Suhling, J., Jaeger, R., Lall, P., Measurement of Die Stresses in Microprocessor Packaging Due to Thermal and Power Cycling, Proceedings of the 62nd ECTC, pp. 756 - 770, 2012
16. Motalab, M., Cai, Z., Suhling, J., Zhang, J., Evans, J., Bozack, M., Lall, P., Improved Predictions of Lead Free Solder Joint Reliability that Include Aging Effects, Proceedings of the 62nd ECTC, pp. 513 - 531, 2012.
17. Lall, P., Narayan, V., Strickland, M., Blanche, J., Suhling, J., Effect of Reflow Process on Glass Transition Temperature of Printed Circuit Board Laminates, Proceedings of the 13th ITherm, pp. 261 – 268, 2012.
18. Chanda, N., Suhling, J., Lall, P., Implementation of a Viscoelastic Model for the Temperature, Proceedings of the 13th ITherm, pp. 269 – 281, 2012.
19. Lall, P., Lowe, R., Goebel, K., Cooper, W., Cost Assessment for Implementation of Embedded Prognostic Health Management for Electronic Systems, Proceedings of the 13th ITherm, pp. 487 – 497, 2012.
20. Lall, P., Gupta, P., Goebel, K., Classification of Multiple Failure Modes in Package-on-Package (PoP) Assemblies using Feature Vectors for Progression of Accrued Damage, Proceedings of the 13th ITherm, pp. 498 – 514, 2012.
21. Lall, P., Sakalaukus, P., Lowe, R., Goebel, K., Leading Indicators for Prognostic Health Management of Electrical Connectors Subjected to Random Vibration, Proceedings of the 13th ITherm, pp. 632 – 638, 2012.
22. Lall, P., Harsha, M., Suhling, J., Goebel, K., Jones, J., Leading Indicator Based Assessment of Operational Readiness in Electronics Subjected To Multiple Environments, Proceedings of the 13th ITherm, pp. 639 – 653, 2012.
23. Lall, P., Limaye, M., Suhling, J., Murtuza, M., Reliability of Lead-free SAC Electronics under Simultaneous Exposure to High Temperature and Vibration, Proceedings of the 13th ITherm, pp. 753 – 761, 2012.
24. Muhannad, M., Cai, Z., Roberts, J., Suhling, J., Lall, P., Evolution of the Tension/Compression and Shear Cyclic Stress-Strain Behavior of Lead Free Solder Subjected to Isothermal Aging, Proceedings of the 13th ITherm, pp. 765 – 780, 2012.
25. Cai, Z., Suhling, J., Lall, P., Bozack, M., Mitigation of Lead Free Solder Aging Effects using Doped SAC-X Alloys, Proceedings of the 13th ITherm, pp. 896 – 909, 2012.
26. Motalab, M., Cai, Z., Suhling, J., Lall, P., Determination of Anand Constants for SAC Solders using Stress-Strain or Creep Data, Proceedings of the 13th ITherm, pp. 909– 921, 2012.
27. Roberts, J., Hussain, S., Suhling, J., Jaeger, R., Lall, P., Characterization of Die Stresses in Microprocessor Packages Subjected to Thermal Cycling, Proceedings of the 13th ITherm, pp. 1003– 1014, 2012
28. Lall, P., Patel, K., Lowe, R., Strickland, M., Blanche, J., Geist, D., Montgomery, R., High-G Shock Reliability of Ceramic Area-Array Packages, Proceedings of the 13th ITherm, pp. 1028– 1036, 2012.
29. Lall, P., Shantaram, S., Suhling, J., Locker, D., Mechanical Deformation Behavior of SAC305 at High Strain Rates, Proceedings of the 13th ITherm, pp. 1037– 1051, 2012.

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