



AUBURN UNIVERSITY

SAMUEL GINN
COLLEGE OF ENGINEERING

Fall 2013

cave³ News

NSF-CAVE3 Electronics Research Center

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INSIDE

- 1 Message from Director
- 2 CAVE³ Review
- 3-8 Research Highlights
- 9-10 Announcements
- 11 Selected Publications

Mission Statement

CAVE is dedicated to working with industry in developing and implementing new technologies for the packaging and manufacturing of electronics, with special emphasis on the cost, harsh environment, and reliability requirements of the automotive, aerospace, military, computing, portable and other industries.

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Message from Director



The escalation of gold prices worldwide has the IC manufacturers scrambling for alternatives for the widely used gold wire for wire bonding. One of the alternatives is the copper wirebonding, which requires conversion of the existing gold wirebonding equipment but has the promise of significant cost savings in lower part costs. For high I/O count parts, transition to

copper wire has the potential of reducing wire costs by up to 90%. Major wire manufacturers have shown increase in copper bonding wire shipments while gold and aluminum bonding wire shipments have stayed flat. Reliability of the copper-aluminum wirebond system is not well understood. Copper has several concerns including corrosion of the IMC layers which may expand in volume causing an open circuit. Control of the pH and Cl- content in the mold compound is critical to Cu-Al wirebond reliability. CAVE3 is working on understanding the fundamental failure mechanisms related to copper wirebonding.

A second major area of focus for CAVE3 is LED technology. LED technology has the potential of making a major positive impact on the environment in more ways than one. Incumbent energy efficient technology choice of CFL contains mercury. According to lightbulbrecycling.com, each year an estimated 600 million fluorescent lamps are disposed of in landfills amounting to 30,000 pounds of mercury waste. The impact on the environment is severe, given that mercury for one fluorescent lamp can pollute several thousand gallons of water beyond safe drinking levels.

LED lighting is expected to increase very rapidly in the coming 10 years according to a survey by

McKinsey & Company with backlighting, general lighting and automotive being major contributors. High cost is one of the significant impediments to the widespread adoption of LED technology. According to the US DOE R&D Roadmap published in August 2012, the packaging materials contribute between 30-60% of the total luminaire. Thus, the packaging materials are key contributors to making the SSL technology more affordable in the future. Further, there is a void in the accelerated test methods available for reliability evaluation of SSLs. Solid state luminaires consist of several length scales with different failure modes at each level. The interactions between optics, drive electronics, controls and thermal design drive the performance of the overall system. Accelerated testing for one sub-system may be too harsh for another sub-system. New methods are needed for predicting the SSL reliability for new and unknown failure modes. LED failure is often addressed by the L70 lifetime. The L70 life is computed based on the minimum 6000 hours of LED testing using the LM-80 and the TM-21 extrapolations of LM-80 data. The TM-21 relies on an exponential model of the LED degradation for the L70 life computation which may not capture the failure physics in presence of multiple failure mechanisms. Weighted average activation energy is based on the large population statistics for a particular LED which may not be applicable. CAVE3 is working on a new methodology for the L70 life prediction of LEDs based on use of the underlying physics models in conjunction with the Kalman Filter.

I want to take this opportunity to welcome Schlumberger to the CAVE3 Consortium.

- Pradeep Lall, T. Walter Professor and Director



CAVE³ Review

CAVE³ Consortium Fall-2013 Technical Review Meeting

The Center for Advanced Vehicle and Extreme Environment Electronics (CAVE³) will hold its Fall Technical Review and Project Planning Meeting on September 11-12, 2013 in Auburn University Wiggins Hall. All current members of the Consortium are invited to attend. The agenda for this event is available at cave.auburn.edu under CAVE³ Reviews. The following projects will be presented at the meeting:

- Acceleration Factors and Life Prediction Models for on-chip and off-chip Failure Mechanisms
- Advanced Interconnect Systems and 3D-Packaging Architectures in Harsh Environments
- Prognostic Health Monitoring Methodologies for Damage Estimation in Lead and Lead-Free Solder Alloys
- PHM for Field-Deployed Electronics Subjected to Multiple Thermal Environments
- Leadfree Part Reliability, Crack Propagation and Life Prediction under Extreme Environments
- The Effects of Environmental Exposure on Underfill Behavior and Flip Chip Reliability
- Models for Underfill Stress-Strain and Failure Behavior with Aging Effects
- In situ Die Stress Measurements in Flip Chip Packaging
- Modeling and Material Characterization for Flip Chip Packaging
- Theoretical and Experimental Investigation on Fretting Corrosion and Thermal Degradation for Hybrid and Electric Vehicles
- Complaint Pin/Press Fit Technology
- Model Simulation and Validation for Vibration-Induced Fretting Corrosion
- Vibration Based Interfaces for Information Transmission
- Microstructural and Mechanical Studies of SAC/Sn-37Pb Mixed Solders
- Aging Behavior of Next Generation Pb-Free Alloys
- Extreme Low Temperature Behavior of Solders
- Composition, Microstructure, and Reliability of Mixed Formulation Solder Joints
- QFP Reliability on Powered and Non-powered Thermal Cycle Environment
- Harsh Environment Substrate Performance
- Module Overmolding for Harsh Environments
- Systems Reliability of Lead Free for Harsh Environment Electronics

A block of rooms has been reserved for Review attendees at the preferred group rate. Room block will expire on September 1, 2013.

Contact Information:

Auburn University Hotel & Conference Center
241 South College Street

SPECIAL EVENTS

AIMS (Harsh Environments Symposium)

Fort Worth Convention Center, Fort Worth, TX
Organized by John Evans and Pradeep Lall

Monday, October 14, 2013
8:00am—5:00pm

This symposium will address the concerns related to harsh environment electronics and the challenges within the electronics community, with an added emphasis on military and space. It is intended to bring together the needs of “end-users” with the capabilities of the research community and the industrial supply base. Specifically, the symposium addresses the challenges of meeting expanding temperature ranges (-55°C to +150°C/+200°C) with increased vibration, higher package density and longer reliability. Next generation requirements are explored from the system level and potential supply-based solutions are presented.

HE1: Thermal Issues with Harsh Environment Electronics

Chair: John Evans, Ph.D., Auburn University

Co-Chair: Charles Bauer, Ph.D., TechLead Corporation

Monday, October 14 | 8:30am — 10:15am | Room 202A

◇ **Thermal Management for FPGAs and 3D Stacks for Space Applications**

Reza Ghaffarian, Ph.D., Jet Propulsion Laboratory

◇ **Improved Prediction of Compressive Forces Required in Thermal Interface Pad Applications**

Jeff Jennings, Harris Corporation

◇ **New Interconnection for High Temperature Application: HotPowCon (HPC)**

Jörg Trodler, Heraeus Materials Technology GmbH & Co.KG, and Robert Bosch, A. Fix, and Mathias Nowotnick, University of Rostock

HE2: Modeling & Predictions in Harsh Operational Envs

Chair: Tom Borkes, The Jefferson Project

Co-Chair: Mike Nadreau, Henkel Electronic Materials LLC

Monday, October 14 | 10:30am — 12:00pm | Room 202A

◇ **A Pseudo-Stress, Pseudo-Strain Methodology to Predict Lead-Free Solder Joint Reliability**

*Jean Paul Clech, Ph.D., EPSI, Inc.

◇ **Life Prediction of Lead-Free Electronics Under Simultaneous Automotive Environments of High Temperature & Vibration**

*Pradeep Lall, Ph.D., M.B.A., Geeta Limaye, Auburn University

◇ **Design for Reliability with Computer Modeling**

*Randy Schueller, Ph.D., DfR Solutions

More information regarding the AIMS Symposium is available at cave.auburn.edu under Workshops

Research Highlights

Cu-Al Wire Bonding Failure Mechanisms

Wire bonding is predominant mode of interconnect in electronics packaging. Traditionally material used for wire bonding is gold. But industry is slowly replacing gold wire bond by copper-aluminum wire bond because of the lower cost and better mechanical properties than gold, such as high strength, high thermal conductivity etc. Numerous studies have been done to analyze failure mechanism of Cu-Al wire bonds. Cu-Al interface is a predominant location for failure of the wirebond interconnects.



Figure 1: X-ray Image – Top view

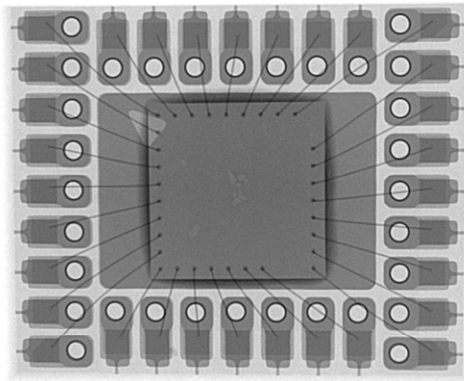


Figure 2 : X-ray Image – Top view

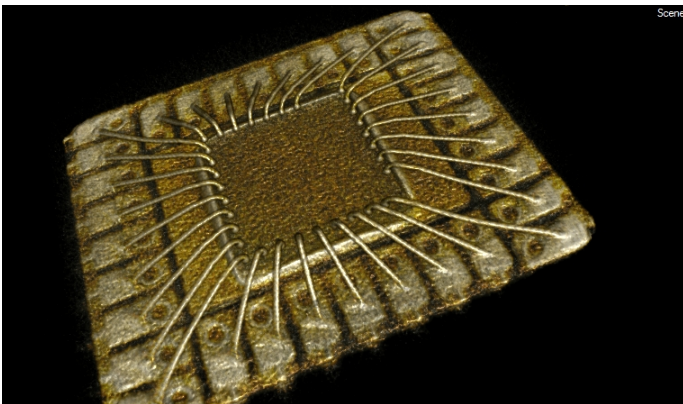


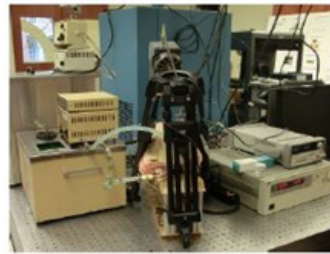
Figure 3 : 3D μ CT Image of 32-pin CSP showing Copper-Aluminum Wirebonds

In this research, the use of intermetallic thickness as leading indicator-of-failure for prognostication of remaining useful life for Cu-Al wire bond interconnects has been studied. For analysis, 32 pin chip scale packages were used. Packages were aged isothermally at 200°C and 250°C for 10 days. Packages were withdrawn periodically after 24 hours and its IMC thickness was measured using SEM. The

parts have been prognosticated for accrued damage and remaining useful life in current or anticipated future deployment environment. The presented methodology uses evolution of the IMC thickness in conjunction with the Levenberg-Marquardt Algorithm to identify accrued damage in wire bond subjected to thermal aging. The proposed method can be used for equivalency of damage accrued in Cu-Al parts subjected to multiple thermal aging environments.

TIM Selection for an IGBT Cold Plate Using Experimental and Numerical Modeling

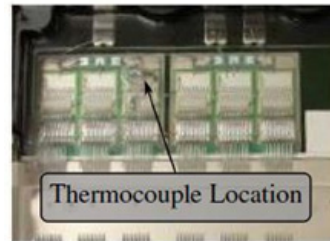
Experimental measurements were used in conjunction with a numerical model to perform an in situ analysis of an IGBT cooling solution with a cold plate utilizing an 85-90°C ethylene glycol-water mixture as the cooling fluid. This process was used to aid in the selection of an appropriate thermal interface material (TIM) for the application. The effects of elevated temperature and thermal cycling on the performance of the TIM were investigated during the selection procedure. Applying the thermal grease with the cold plate at 70°C rather than 30°C caused a reduction in the junction to case resistance of 74% and 78% for the two thermal greases tested.



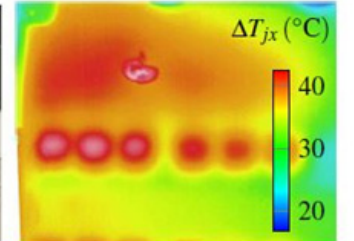
(a) experimental setup



(b) thermocouple inserted through lid



(c) photograph of thermocouple location



(d) thermal image of IGBT module operating at 250W

Figure 4: Experimental Setup to Power IGBT Module and Measure the Temperature of the Silicon Devices.

PoP Warpage Prediction and Control

Package-on-Package (PoP) assemblies may experience warpage during package fabrication and later during surface mount assembly. Excessive warpage may result in loss-of-coplanarity, open connections, mis-shaped joints, and reduction in package board-level reliability (BLR) under environmental stresses of thermal cycling, shock and vibration. Previous researchers have shown that

Research Highlights

warpage may be influenced by a number of design and process factors including underfill properties, mold properties, package geometry, package architecture, board configuration, underfill and mold dispense and cure parameters, package location in the molding panel. A comprehensive inverse model incorporating a full set of design and process parameters and their effect on PoP package and PoP assembly warpage is presently beyond the state of art.

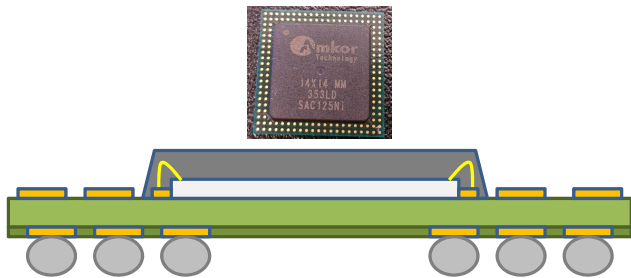


Figure 5: Test vehicle 1 package architecture

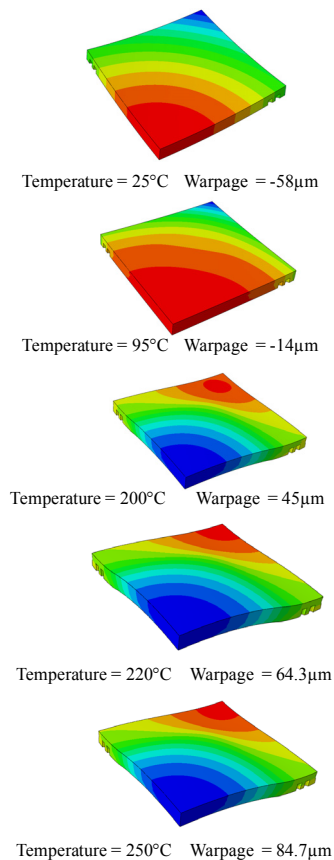


Figure 6: Warpage at key temperatures

In this research, data has been gathered on multiple package-on-package assemblies under a variety of assembly parameters. The packages have been speckle coated. The warpage of the PoP assemblies have been measured using a glass-top reflow oven using multiple cameras. Warpage measurements have been taken at various tem-

perature of the reflow profile between room temperature and the peak reflow temperature. Finite element models have been created and the package-on-package warpage predictions have been correlated with the experimental data. The experimental data-set has been augmented with the simulation data to evaluate configurations and parameter-variations which were not available in the experimental dataset. Statistical models have been developed to capture the effect of single and multiple parameter variations using principal components regression, and ridge regression. Best subset variables obtained from stepwise methods, have been used for model development. The developed models have been validated with experimental data using a single factor design of experiment study and are found to accurately capture material and geometry effects on part warpage. The results show that the proposed approach has the potential of predicting both single and coupled factor effects on warpage.

Correlation of Reliability Models Including Aging Effects with Thermal Cycling Reliability Data

The microstructure, mechanical response, and failure behavior of lead free solder joints in electronic assemblies are constantly evolving when exposed to isothermal aging and/or thermal cycling environments. Traditional finite element based predictions for solder joint reliability during thermal cycling accelerated life testing are based on solder constitutive equations (e.g. Anand viscoplastic model) and failure models (e.g. energy dissipation per cycle model) that do not evolve with material aging. Thus, there will be significant errors in the calculations with lead free SAC alloys that illustrate dramatic aging phenomena.

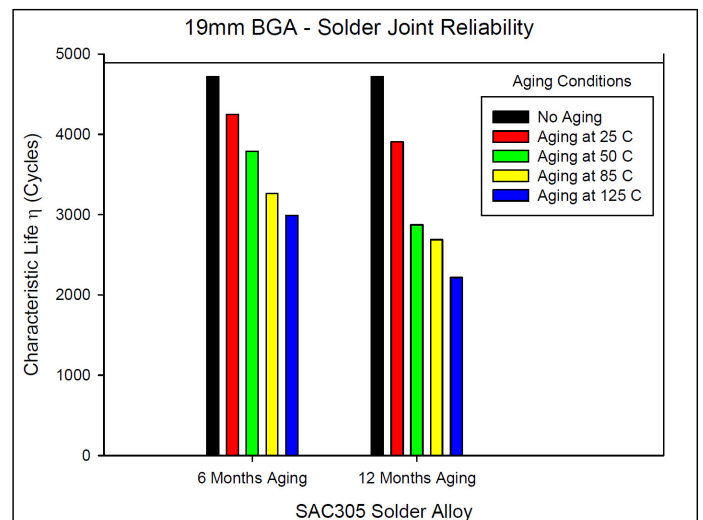


Figure 7: Effects of Aging on Characteristic Life.

In this research, we have developed a new reliability prediction procedure that utilizes constitutive relations and failure criteria that incorporate aging effects, and then validated the new approach through correlation with thermal cycling accelerated life testing experimental data. As a part of this work, a revised set off Anand

Research Highlights

viscoplastic stress-strain relations for solder have been developed that included material parameters that evolve with the thermal history of the solder material. The effects of aging on the nine Anand model parameters have been determined as a function of aging temperature and aging time, and the revised Anand constitutive equations with evolving material parameters have been implemented in commercial finite element codes. In addition, new aging aware failure criteria have been developed based on fatigue data for lead free solder uniaxial specimens that were aged at elevated temperature for various durations prior to mechanical cycling. Using the measured fatigue data, mathematical expressions have been developed for the evolution of the solder fatigue failure criterion constants with aging, both for Coffin-Manson (strain-based) and Morrow-Darveaux (dissipated energy based) type fatigue criteria. Similar to the findings for mechanical/constitutive behavior, our results show that the failure data and associated fatigue models for solder joints are affected significantly by isothermal aging prior to cycling. After development of the tools needed to include aging effects in solder joint reliability models, we have then applied these approaches to predict reliability of PBGA components attached to FR-4 printed circuit boards that were subjected to thermal cycling. Finite element modeling was performed to predict the stress-strain histories during thermal cycling of both non-aged and aged PBGA assemblies, where the aging at constant temperature occurred before the assemblies were subjected to thermal cycling. The results from the finite element calculations were then combined with the aging aware fatigue models to estimate the reliability (cycles to failure) for the aged and non-aged assemblies. As expected, the predictions show significant degradations in the solder joint life for assemblies that had been pre-aged before thermal cycling. To validate our new reliability models, an extensive test matrix of thermal cycling reliability testing has been performed using a test vehicle incorporating several sizes of fine pitch PBGA daisy chain components. Before thermal cycling began, the assembled test boards were divided up into test groups that were subjected to several sets of aging conditions (preconditioning) including different aging temperatures ($T = 25, 55, 85$ and 125 C) and different aging times (no aging, and 6 and 12 months). After aging, the assemblies were subjected to thermal cycling (-40 to $+125$ C) until failure occurred. As with the finite element predictions, the Weibull data failure plots have demonstrated that the thermal cycling reliabilities of pre-aged assemblies were significantly less than those of non-aged assemblies. Good correlation was obtained between new reliability modeling procedure and the measured solder joint reliability data.

Predictive Models for Simultaneous Exposure to Temperature and Vibration

Current trends in the automotive industry warrant a variety of electronics for improved control, safety, efficiency and entertainment. Many of these electronic systems like engine control units, variable valve sensor, crankshaft-camshaft sensors are located under-hood. Electronics installed in under-hood applications are subjected simultaneously to mechanical vibrations and thermal loads. Typical failure modes caused by vibration induced high cycle fatigue include solder fatigue, copper trace or lead fracture.

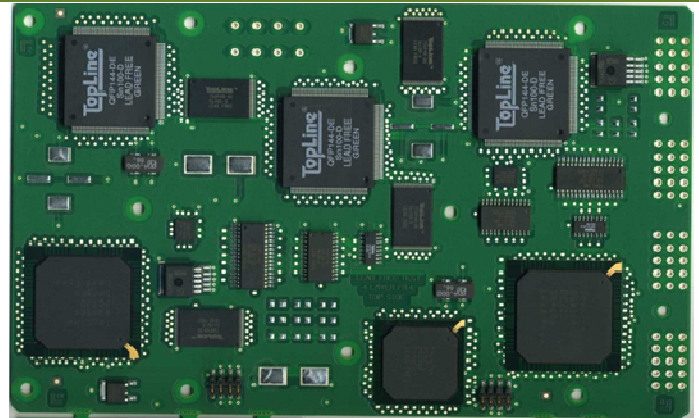


Figure 8: Product form-factor test vehicle

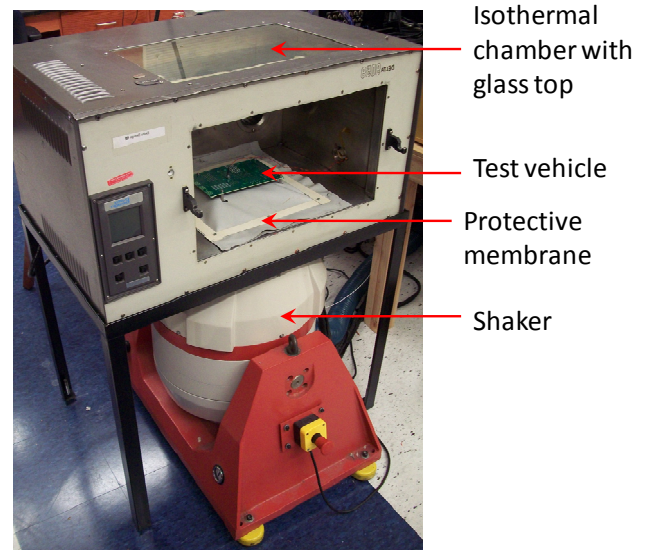


Figure 9: PCB inside the isothermal chamber with electrodynamic shaker.

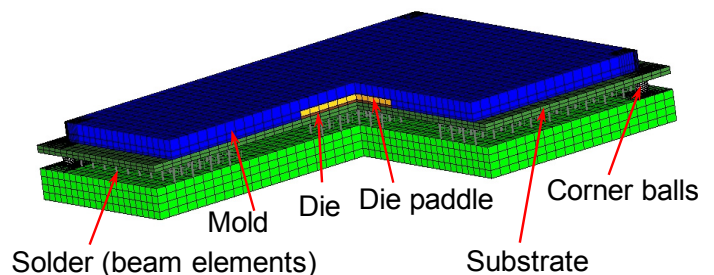


Figure 10: BGA sub-models

Research Highlights

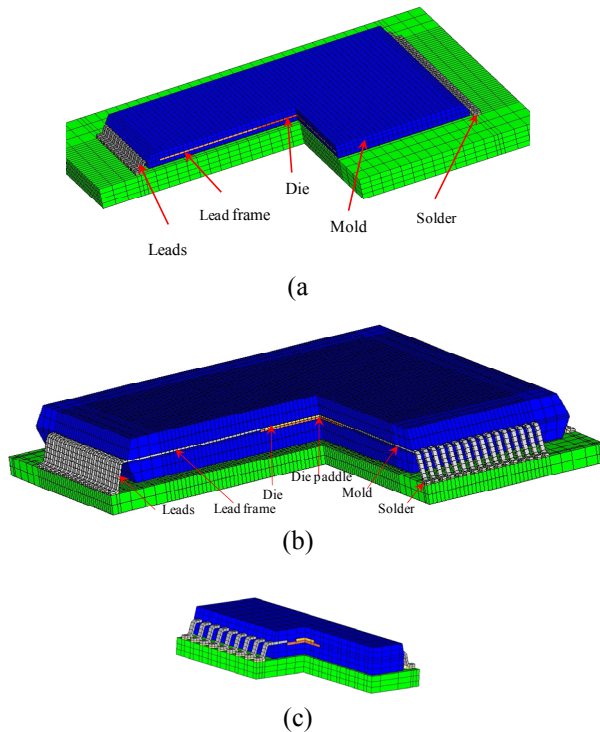


Figure 10: (a) TSOP (b) QFP (c) SOL sub-models

The solder interconnects accrue damage much faster when vibrated at elevated temperatures. Industry migration to lead-free solders has resulted in a proliferation of a wide variety of solder alloy compositions. Presently, the literature on mechanical behavior of lead-free alloys under simultaneous harsh environment of high-temperature vibration is sparse. In this research, the reduction in stiffness of the PCB with temperature has been demonstrated by measuring the shift in natural frequencies. The test vehicle consisting of a variety of lead-free SAC305 daisy chain components including BGA, QFP, SOP and TSOPs has been tested to failure by subjecting it to two elevated temperatures and harmonic vibrations at the corresponding first natural frequency. The test matrix includes three test temperatures of 25°C, 75°C and 125°C and simple harmonic vibration amplitude of 10G which are values typical in automotive testing. PCB deflection has been shown to increase with increase in temperature. The full field strain has been extracted using high speed cameras operating at 100,000 fps in conjunction with digital image correlation. Material properties of the PCB at test temperatures have been measured using tensile tests and dynamic mechanical analysis. FE simulation using global-local finite element models is thus correlated with the system characteristics such as modal shapes, natural frequencies and displacement amplitudes for every temperature. The solder level stresses have been extracted from the sub-models. Stress amplitude versus cycles to failure curves are obtained at all the three test temperatures. A comparison of failure modes for different surface mount packages at elevated test temperatures and vibration has been presented in this study.

Influence of Uniaxial Normal Stress on the Performance of Vertical Bipolar Transistors

In this project, CAVE researchers have explored the response of bipolar junction transistors (BJT) to the controlled application of mechanical stress. Mechanical strains and stresses are developed during the fabrication, assembly and packaging of the integrated circuit (IC) chips. Due to these stresses and strains, it has been observed by many researchers that changes can occur in the electrical performance of both analog and digital devices. Stress-induced device parametric shifts affect the performance of analog circuits that depend upon precise matching of bipolar and/or MOS devices, and can cause them to operate out of specifications. In the past the authors have extensively investigated the stress effects on resistors embedded on integrated chips and were successful in characterizing die stresses for various packaging architectures. We have also observed stress effects on diodes, field effect transistors (FETs), van der Pauw structures and CMOS sensor arrays. In this present work, the stress dependence of the electrical behavior of bipolar transistors has been investigated.

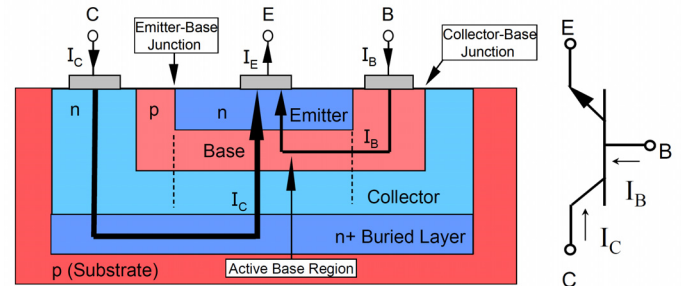


Figure 11: Simplified Schematic a Vertical npn Bipolar Transistor

Test structures have been utilized to characterize the stress sensitivity of vertical bipolar devices fabricated on (100) silicon wafers. In the experiments, uniaxial normal stresses were applied to silicon wafer strips using a four-point-bending fixture. An approximate theory has also been developed for stress-induced changes in the current gain of bipolar junction transistors. Both the theoretical and experimental results show similar trend for DC current gain vs. stress plots. Multi-Physics based finite element simulations (coupled electro-mechanical-thermal) have been performed to understand the device level mechanisms that cause the stress induced changes in the BJTs and also to characterize and model stress dependence of fundamental silicon material parameters such as bandgap, intrinsic carrier concentration, and electron/hole mobilities. In the future, the developed formulations can be applied to theoretically optimize transistor design, placement, orientation, and processing to minimize the impact of fabrication and packaging induced die stresses.

High Strain Rate Properties of Innolot™

Industry migration to lead-free solders has resulted in a proliferation of a wide variety of solder alloy compositions. The most popular amongst these are the Tin-Silver-Copper (Sn-Ag-Cu or SAC) fami-

Research Highlights

ly of alloys like SAC105, SAC305 etc. Recent studies have highlighted the detrimental effects of isothermal aging on the material properties of these alloys. SAC alloys have shown up to 50% reduction in their initial elastic modulus and ultimate tensile strength within a few months of elevated temperature aging. This phenomenon has posed a severe design challenge across the industry and remains a road-block in the migration to Pb-free. Multiple compositions with additives to SAC have been proposed to minimize the effect of aging and creep while maintaining the melting temperatures, strength and cost at par with SAC. Innolot is a newly developed high-temperature, high-performance lead-free substitute by InnoRel™ targeting the automotive electronics segment. Innolot contains Nickel (Ni), Antimony (Sb) and Bismuth (Bi) in small proportions in addition to Sn, Ag and Cu. The alloy has demonstrated enhanced reliability under thermal cycling as compared to SAC alloys. In this paper, the high strain rate material properties of Innolot have been evaluated as the alloy ages at an elevated temperature of 50°C. The strain rates chosen are in the range of 1-100 per-second which are typical at second level interconnects subjected to drop-shock environments. The strain rates and elevated aging temperature have been chosen also to correspond to prior tests conducted on SAC105 and SAC305 alloys at this research center. This research effort presents a comparison of material properties and their degradation in the three alloys – SAC105, SAC305 and Innolot. Full field strain measurements have been accomplished with the use of high speed imaging in conjunction with Digital Image Correlation (DIC). Ramberg-Osgood non-linear model parameters have been determined to curve-fit through the experimental data. The parameters have been implemented in Abaqus FE model to obtain full-field stresses which correlates with contours obtained experimentally by DIC.

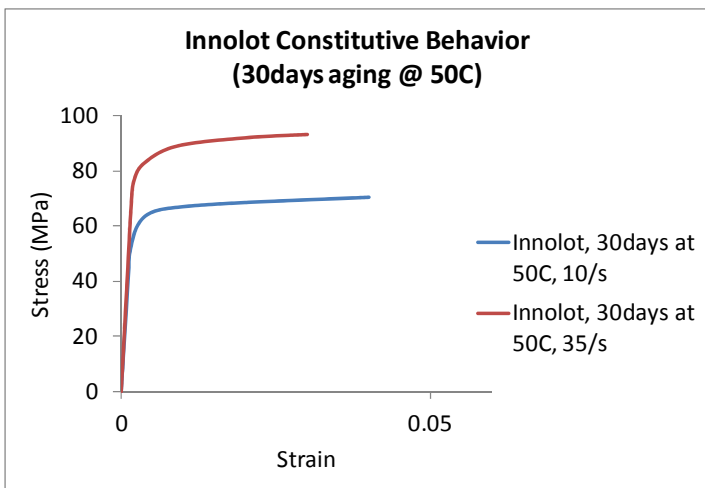


Figure 12: Stress-strain curves for Innolot aged at 50C for 30 days

Solid State Luminaires Under HTSL

This research will show an investigation of off-the-shelf luminaires with the focus on the LED electronic drivers, specifically the aluminum electrolytic capacitors (AECs), that have been aged using high temperature shelf life (HTSL) testing of 135°C in order to prognos-

ticate the remaining useful life of the luminaires. Luminaires have the potential of seeing excessive temperatures when being transported across the country or being stored in non-climate controlled warehouses. They are also being used in outdoor applications in desert environments that see little or no humidity but will experience extremely high temperatures during the day. This makes it important to increase our understanding of what effects being stored at high temperatures for a prolonged period of time will have on the usability and survivability of these devices.

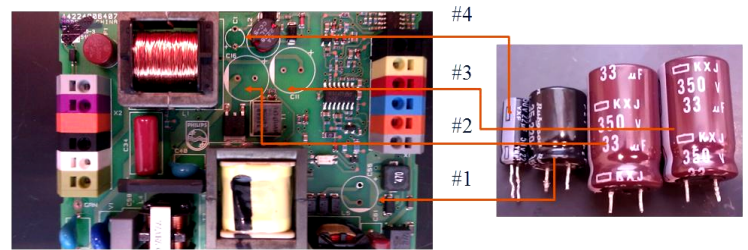


Figure 13: AECs Removed from the Philips Xitanium Driver.

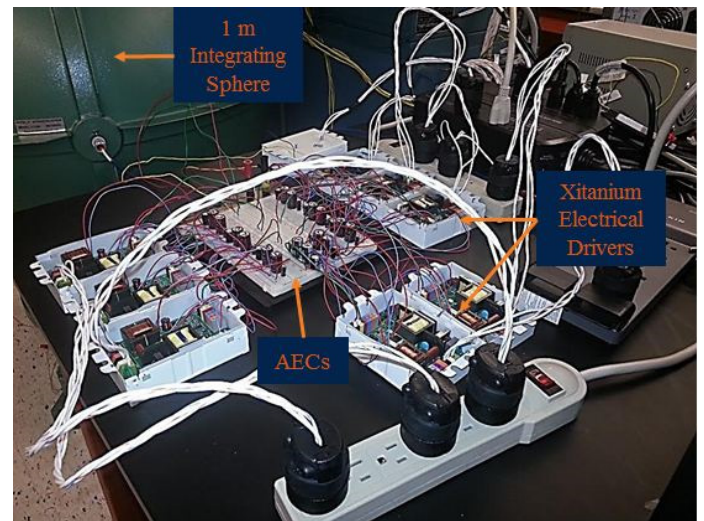


Figure 14: Luminous Flux Measurement Setup.

The U.S. Department of Energy has made a long term commitment to advance the efficiency, understanding and development of solid-state lighting (SSL) and is making a strong push for the acceptance and use of SSL products. In this work, the four AECs of three different types inside each LED electronic driver were studied. The change in capacitance and the change in equivalent series resistance (ESR) of the AECs were measured and considered to be a leading indication of failure of the LED system. These indicators were used to make remaining useful life predictions to develop an algorithm to predict the end of life of the AECs. The luminous flux of a pristine downlight module was also monitored using each LED electronic driver that was subjected to HTSL through the progression of the testing to determine a correlation between the light output of the lamp and the failing components of the LED electronic driver. Prognostic and Health Management (PHM) is a useful tool for as-

Research Highlights

assessment of the remaining life of electrical components and is demonstrated for AECs in this work.

LED L70 Life Prediction

Solid-state lighting (SSL) luminaires containing light emitting diodes (LEDs) have the potential of seeing excessive temperatures when being transported across country or being stored in non-climate controlled warehouses. They are also being used in outdoor applications in desert environments that see little or no humidity but will experience extremely high temperatures during the day. This makes it important to increase our understanding of what effects high temperature exposure for a prolonged period of time will have on the usability and survivability of these devices. The U.S. Department of Energy has made a long term commitment to advance the efficiency, understanding and development of solid-state lighting (SSL) and is making a strong push for the acceptance and use of SSL products to reduce overall energy consumption attributable to lighting. Traditional light sources “burn out” at end-of-life. For an incandescent bulb, the lamp life is defined by B50 life. However, the LEDs have no filament to “burn”.

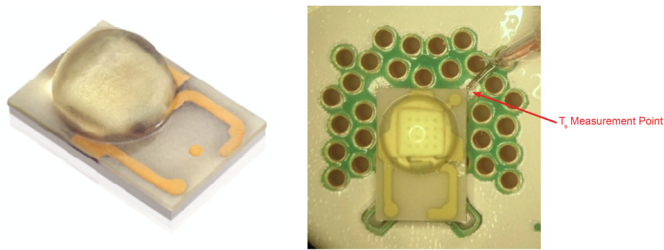


Figure 15: LED Test Product

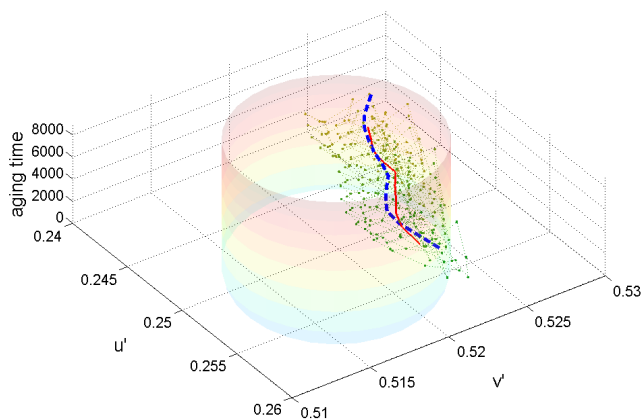


Figure 16 KF Chromaticity Tracking

The LEDs continually degrade and the light output decreases eventually below useful levels causing failure. Presently, the methods described in IES TM-21 are used to predict the L70 life of white LEDs from LM-80 test data. Several failure mechanisms may be active in a LED at a single time causing lumen depreciation. The underlying TM-21 Arrhenius Model may not capture the failure

physics in presence of multiple failure mechanisms. Correlation of lumen maintenance with underlying physics of degradation at system-level is needed. In this research, a Kalman Filter and Extended Kalman Filters (EKF) have been used to develop a 70% Lumen Maintenance Life Prediction Model for LEDs used in SSL luminaires. This model can be used to calculate acceleration factors, evaluate failure-probability and identify ALT methodologies for reducing test time. Nine-thousand hour LM-80 test data for various LEDs have been used for model development. System state has been described in state space form using the measurement of the feature vector, velocity of the feature vector change and the acceleration of the feature vector change. System state at each future time has been computed based on the state space at preceding time step, system dynamics matrix, control vector, control matrix, measurement matrix, measured vector, process noise and measurement noise. The future state of the lumen depreciation has been estimated based on a second order Kalman Filter model and a Bayesian Framework. The measured state variable has been related to the underlying damage using physics-based models. Life prediction of L70 life for the LEDs used in SSL luminaires from KF and EKF based models have been compared with the TM-21 model predictions and experimental data.

Role of Incorporated Hydrogen on Tin Whiskering.

The role of incorporated hydrogen on the growth of tin (Sn) whiskers is currently unknown, despite suspicions for years that it plays a role in whisker incubation and growth processes. The presence of hydrogen is of particular concern for electrodeposited films, where the plating bath contains considerable amounts of hydrogen-containing molecules which are incorporated into the deposited thin film. In this work we have investigated the role of hydrogen in whiskering by implanting a high dose, uniform distribution ($\sim 2 \times 10^{19}/\text{cm}^3$) of 550 keV protons into ~ 1.5 micron sputtered Sn films (on Si) by a particle accelerator. Prior to the implant, the Sn films were deposited under both tensile and compressive intrinsic stress conditions and each specimen had an implanted and (masked, control) non-implanted side. Results to date indicate no significant differences in whisker number densities between implanted and non-implanted film regions. Details will be reported at the 2013 IEEE Holm Conference on Electrical Contacts (Newport, R.I.) in September.

Characterization of Aging Effects in Lead Free Solder Joints Using Nanoindentation

The mechanical properties of a lead free solder are strongly influenced by its microstructure, which is controlled by its thermal history including solidification rate and thermal aging after solidification. Due to aging phenomena, the microstructure, mechanical response, and failure behavior of lead free solder joints in electronic assemblies are constantly evolving when exposed to isothermal and/or thermal cycling environments. Through uniaxial testing of miniature bulk older tensile specimens, we have previously demonstrated that large changes occur in the stress-strain and creep behaviors of lead free solder alloys with aging. Complementary studies by other research groups have verified aging induced degradations of SAC

Research Highlights

mechanical properties. In those investigations, mechanical testing was performed on a variety of sample geometries including lap shear specimens, Iosipescu shear specimens, and custom solder ball array shear specimens. While there are clearly aging effects in SAC solder materials, there have been limited prior mechanical loading studies on aging effects in actual solder joints extracted from area array assemblies (e.g. PBGA or flip chip). This is due to the extremely small size of the individual joints, and the difficulty in gripping them and applying controlled loadings (tension, compression, or shear). In the current work, we have explored aging phenomena in actual solder joints by nano-mechanical testing of single SAC305 lead free solder joints extracted from PBGA assemblies. Using nanoindentation techniques, the stress/strain and creep behavior of the SAC solder materials have been explored at the joint scale for various aging conditions. Mechanical properties characterized as a function of aging include the elastic modulus, hardness, and yield stress.

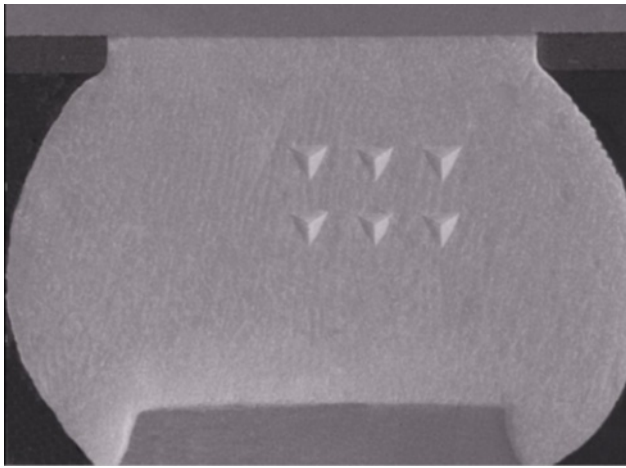


Figure 17 : Solder Ball after Nanoindentation Testing.

Using a constant force at max indentation, the creep response of the aged and non-aged solder joint materials has also been measured as a function of the applied stress level. With these approaches, aging effects in solder joints were quantified and correlated to the magnitudes of those observed in testing of miniature bulk specimens. Our results show that the aging induced degradations of the mechanical properties (modulus, hardness) of single grain SAC305 joints were similar to those seen previously by testing of larger “bulk” solder specimens. However, due to the single grain nature of the joints considered in this study, the degradations of the creep responses were significantly less in the solder joints relative to those in larger uniaxial tensile specimens. The magnitude of aging effects in multi-grain lead free solder joints remains to be quantified. Due to the variety of crystal orientations realized during solidification, it was important to identify the grain structure and crystal orientations in the tested joints. Polarized light microscopy and Electron Back Scattered Diffraction (EBSD) techniques have been utilized for this purpose. The test results show that the elastic, plastic, and creep properties of the solder joints and their sensitivities to aging are highly dependent on the

crystal orientation. In addition, an approach has been developed to predict tensile creep strain rates for low stress levels using nanoindentation creep data measured at very high compressive stress levels.

The Effects of Aging of the Cyclic Stress-Strain and Fatigue Behaviors of Lead-free Solders

Solder joints in electronic assemblies are typically subjected to thermal cycling, either in actual application or in accelerated life testing used for qualification. Mismatches in the thermal expansion coefficients of the assembly materials cause the solder joints to be subjected to cyclic (positive and negative) mechanical strains and stresses. This cyclic loading leads to thermo-mechanical fatigue damage that involves damage accumulation, crack initiation, crack propagation, and failure. In addition, the microstructure, mechanical response, and failure behavior of lead free solder joints in electronic assemblies are constantly evolving when exposed to isothermal aging and/or thermal cycling environments. While the effects of aging on solder constitutive behavior (stress-strain and creep) have been examined in some detail, there have been no prior studies on the effects of aging on solder failure and fatigue behavior. Aging leads to both grain and phase coarsening, and can cause recrystallization at Sn grain boundaries. Such changes are closely tied to the damage that occurs during cyclic mechanical loading. In this investigation, we have examined the effects of aging on the cyclic stress-strain behavior and fatigue life of lead free solders.

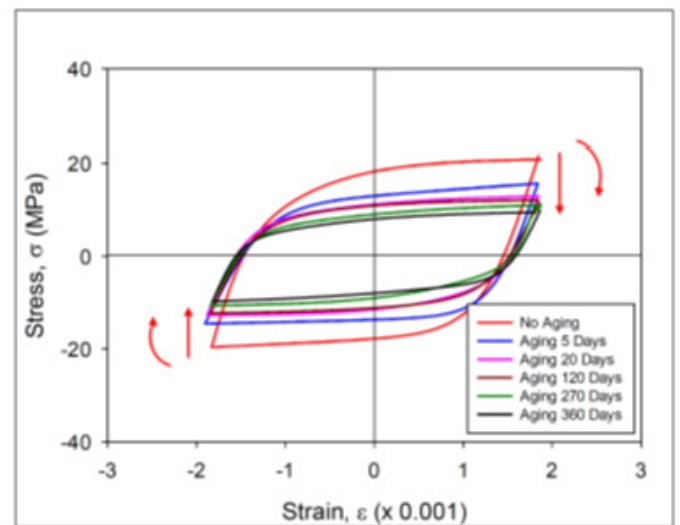


Figure 18: Hysteresis Loops for Cyclic Stress-Strain Testing of SAC105 (Strain Controlled, Aging for 0-12 Months at 125°C)

Uniaxial solder test specimens (SAC105 and SAC305) have been prepared and subjected to cyclic stress/strain loading at different aging conditions. A four-parameter hyperbolic tangent empirical model has been used to fit the entire cyclic stress-strain curve and the hysteresis loop size (area) was calculated using definite integration for a given strain limit. This area represents the energy dissipated per cycle, which is correlated to the damage accumulation in the

Research Highlights

joint. Using the recorded cyclic stress-strain curves, the evolution of the solder hysteresis loops with aging have been characterized and empirically modeled. Similar to solder stress-strain and creep behavior, there is a strong effect of aging on the hysteresis loop size (and thus the rate of damage accumulation) in the solder specimens. Fatigue experiments were also performed, where the uniaxial specimens were subjected to cyclic loading over a particular strain range until failure. Fatigue failure in the experiments was defined to occur when there was a 50% peak load drop during mechanical cycling. Prior to testing, the specimens were aged (preconditioned) at 125 °C for various aging times, and then the samples were subjected to cyclic loading at room temperature (25 °C). It was found that aging decreased the mechanical fatigue life, and the effects of aging on the peak load drop have been studied. It has also been observed that degradations in the fatigue/failure behavior of the lead free solders with aging are highly accelerated for lower silver content alloys (e.g., SAC105). Various empirical failure criteria such as the Coffin-Manson model and the Morrow model have been used to fit the measured data, and the parameters in the models have been determined as a function of the aging conditions.

Measurement of Microprocessor Die Stress Due to Thermal Cycling, Power Cycling and Second Level Assembly

In the current work, we have extended our past studies on Flip Chip Ceramic Ball Grid Array (FC-BGA) microprocessor packaging configurations to investigate in-situ die stress variation during thermal and power cycling. The utilized (111) silicon sensor rosettes were able to measure the complete three-dimensional stress state (all 6 stress components) at each sensor site being monitored by the data acquisition hardware. The test chips had dimensions of 20 x 20 mm, and 3600 lead free solder interconnects (full area array) were used to connect the chips to high CTE ceramic chip carriers.

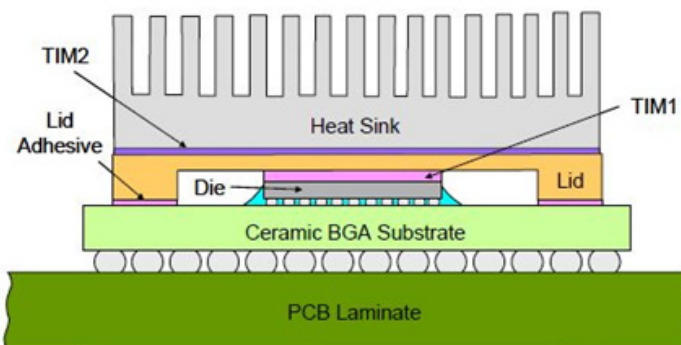


Figure 19: Typical Packaging Architecture for a High Performance Flip Chip Microprocessor.

A unique package carrier was developed to allow measurement of the die stresses in the FCCBGA components under thermal and power cycling loads without inducing any additional mechanical loadings. Initial experiments consisted of measuring the die stress levels while

the components were subjected to a slow (quasistatic) temperature changes from 0 to 100 C. In later testing, long term thermal cycling of selected parts was performed from 0 to 100 C (40 minute cycle, 10 minute ramps and dwells). After various durations of cycling, the sensor resistances at critical locations on the die device surface (e.g. die center and die corners) were recorded. From the resistance data, the stresses at each site were calculated and plotted versus time. Finally, thermal and power cycling of selected parts was performed, and in-situ measurements of the transient die stress variations were performed. Power cycling was implemented by exciting the on-chip heaters on the test chips with various power levels. During the thermal/power cycling, sensor resistances at critical locations on the die device surface (e.g. die center and die corners) were recorded continuously. From the resistance data, the stresses at each site were calculated and plotted versus time.

Impact of High Temperature Storage on Reliability of Leadfree Electronics

Electronic systems may be subjected to prolonged and intermittent periods of storage prior to deployment or usage. Prior studies have shown that leadfree solder interconnects show measurable degradation in the mechanical properties even after brief exposures to high temperature. In this research, a method has been developed for the determining equivalent storage time to produce identical damage at a different temperature. Electronics subjected to accelerated tests often have a well-defined thermal profile for a specified period of time. Quantification of the thermal profile in field deployed electronics may be often difficult because of variance in the environment conditions and usage profile. There is need for tools and techniques to quantify damage in deployed systems in absence of macro-indicators of damage without knowledge of prior stress history.

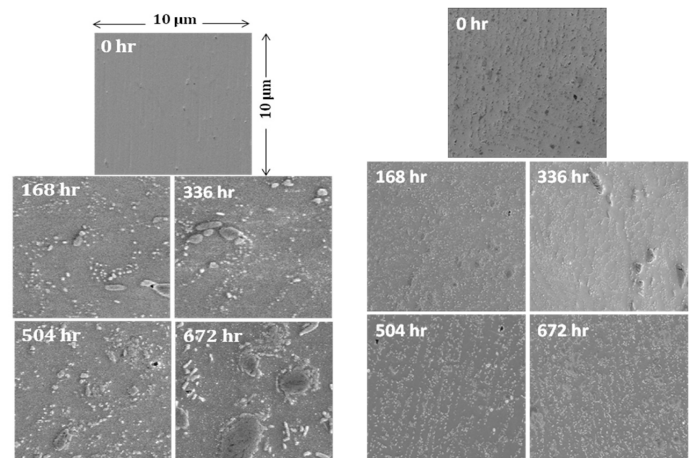


Figure 20: Phase Growth in CABGA 36 and CABGA 256 under 60C Exposure

High reliability applications such as avionics and missile systems may be often exposed to long periods of storage prior to deployment. Effect of storage at different temperature conditions can be mapped using the presented approach.

Announcements

Lall Receives the SEC Faculty Achievement Award

Auburn University and the Southeastern Conference announced that Professor Pradeep Lall of the Samuel Ginn College of Engineering has been honored with the SEC's Auburn University Faculty Achievement Award for 2012-2013. Lall will receive a \$5,000 honorarium. The SEC Faculty Achievement Awards, created to recognize faculty accomplishments, scholarly contributions and discoveries, were established by the SEC presidents and chancellors and are administered by the SEC provosts. "Dr. Lall is an outstanding faculty member who is truly dedicated to his students, colleagues and his profession," said Timothy Boosinger, Auburn University provost and vice president for academic affairs. "His work is exceptional and we are pleased to recognize his accomplishments." "The SEC Faculty Achievement Awards provide an opportunity for each SEC university to showcase the strengths of its faculty, who excel in many disciplines with varying areas of expertise," said Jay Gogue, president of Auburn University and president of the Southeastern Conference. "I am truly honored and humbled to receive the SEC Faculty Achievement Award, given the esteemed company of faculty at the SEC universities and the stiff competition for this award," Lall said. "The award is a testament to the strong research and education environment at Auburn University that provides students with world-class learning opportunities."

Lall Appointed Representative on IEEE-USA Government Relations Council for Research and Development Policy

Pradeep Lall has been appointed as the IEEE Reliability Society Representative on the IEEE-USA Government Relations Council for Research and Development Policy. The purpose of IEEE-USA's government relations committees (herein Committees), as specified in their charters, is to inform and influence policymakers about policy issues with significant technological content in which IEEE-USA has expertise. Products and activities of the committees include Policy or Position Statements; testimony before executive, legislative or regulatory bodies; meetings with staff members and/or legislators; letters to newspapers or other publications; technology policy symposia; and other activities. The committees perform their work primarily through the efforts of IEEE-USA volunteers, who provide the technical and policy expertise either through their individual abilities or through their liaison with technical societies and regions (through liaison representatives and Technical Information Statements).

CAVE Researchers Receive the Best Paper Award for ECTC 2012 paper at the ECTC 2013, Las Vegas

The following paper presented at the ECTC 2012 by CAVE Researchers received the Best-of-Conference Award at the ECTC 2013: Lall, P., Patel, K., Lowe, R., Strickland, M., Blanche, J., Geist, D., Montgomery, R., Modeling and Reliability Characterization of Area-Array Electronics Subjected to High-G Mechanical Shock Up to 50,000G, Proceedings of the 62nd ECTC, pp. 1194 – 1204, May 29-June 1, 2012.



Pradeep Lall Receiving the Best-of-Conference Paper Award at the ECTC 2013

The CAVE3 Team lead by Prof. Lall has been studying electronic systems in defense aerospace applications which are often required to function under extreme gravitational forces beyond those seen in consumer applications. In this research paper, "Modeling and Reliability Characterization of Area-Array Electronics Subjected to High-G Mechanical Shock up to 50,000G," the CAVE3 team studied the functionality of electronic systems used in aerospace applications during high-gravity events using high-speed video, computational modeling and optical strain measurements. Portable electronics products such as smartphones and tablets which may be accidentally dropped during normal usage often see high-g loads in the neighborhood of 1500 to 3000g. Damage in typical smartphones and tablets may range from broken LCD screens to non-functional products. The gravity loads seen in aerospace applications are significantly higher. In his research, Lall is developing methods to model onset of degradation, dominant failure mechanisms, predict life and improve survivability of electronic systems during high-gravity level events using a unique combination of high-speed video, computational modeling, optical strain measurements and μ CT based non-destructive evaluation. Survivability of electronic assemblies has been studied at extreme-g levels of up to 100,000G. Electronics at such high g-loads may undergo significant transient deformation under the high inertial forces which may damage the electronics components. Designers of electronics systems are continuously searching for new methods for enhancing survivability of these electronic systems. The events are so fast that capturing the damage mechanics often requires camera systems and data acquisition systems capable of operating at very-high speeds. To enable this research, Lall is using shock towers capable of operating at 100,000G of acceleration loading with high speed cameras capable of recording 275,000 frames per second. A normal consumer grade camera may only record images at a slow 30 frames per second.

Announcements



From Left to Right: Yihua Luo, Junchao Wei, Shantanu Deshpande, Pradeep Lall, Peter Sakalaukus, Mahendra Harsha

CAVE Researchers Win Best Paper Awards at the ASME InterPACK 2013, Burlingame, CA

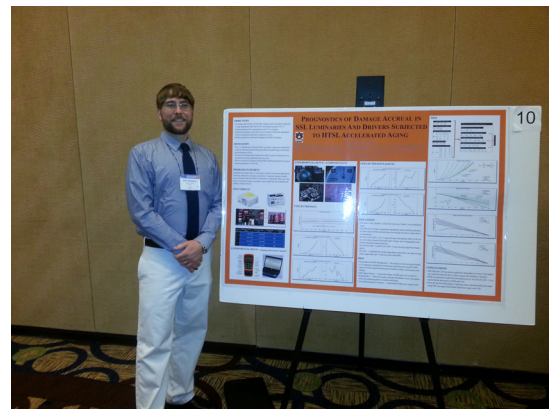
The following paper won awards in the best oral and best poster categories at the ASME InterPACK 2013 Conference:

Best Oral Paper Award: Richard C. Jaeger, Mohammad Motalab, Safina Hussain, Jeffrey C. Suhling, Four-wire bridge measurements of van der pauw Stress sensors on (100) and (111) silicon, Proceedings of the ASME InterPACK, InterPACK2013-73249, pp. 1-17, Burlingame, CA, 2013.

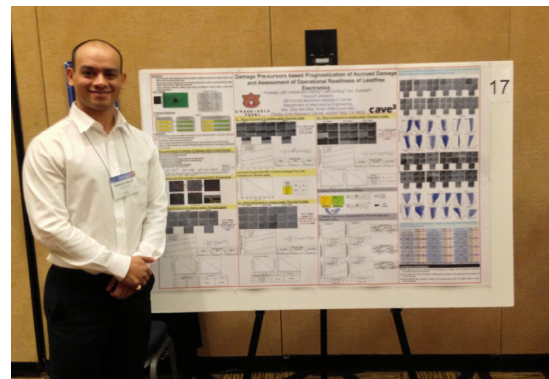
Best Poster Paper Award: Lall, P., Harsha, M., Suhling, J., Goebel, K., Damage Pre-Cursors Based Prognostication of Accrued Damage and Assessment of Operational Readiness of Lead-free Electronics, Proceedings of the ASME InterPACK, InterPACK2013-73251, pp. 1-17, Burlingame, CA, 2013.

Both papers were recognized at the Awards Luncheon at the ASME InterPACK 2013 Conference.

Several students attended the ASME InterPACK 2013 to present papers. In all CAVE3 researchers presented 19 papers at the conference. Students attending the conference included: Shantanu Deshpande, Peter Sakalaukus, Yihua Luo, Mahendra Harsha, Junchao Wei, Mohammad Motalab, Muhannad Mustafa, Munshi Basit, Mohammad Hasnine, Muhannad Mustafa, Jing Zou, Jordan C. Roberts, Nusrat J. Chhanda, John Maddox, and Safina Hussain. Faculty Attending included: Professor(s) Roy Knight, Pradeep Lall and Jeff Suhling.



P. Sakalaukus Presenting Poster titled: Prognostication of Damage Accrued in SSL Luminaires and Drivers Subjected to HTSL



M. Harsha Presenting Poster titled: Damage Precursors and Prognostication of Accrued Damage and Assessment of Operational Readiness of Leadfree Electronics.

Selected Recent Publications

1. Hasnine, M., Mustafa, M., Suhling, J., Prorok, B., Bozack, M., Lall, P., Characterization of Aging Effects in Lead Free Solder Joints Using Nanoindentation, Electronic Components and Technology Conference, ECTC, 63rd, pp.166-178, 2013.
2. Lall, P., Patel, K., Narayan, V., Model for Prediction of Package -on-Package Warpage and the Effect of Process and Material Parameters, Electronic Components and Technology Conference, ECTC, 63rd, pp.608-622, 2013.
3. Lall, P., Mirza, K., Harsha, M., Suhling, J., Goebel, K., Damage Pre-Cursor Based Assessment of Impact of High Temperature Storage on Reliability of Lead-free Electronics, Electronic Components and Technology Conference, ECTC, 63rd, pp.817-826, 2013.
4. Motalab, M., Mustafa, M., Suhling, J., Zhang, J., Evans, J., Bozack, M., Lall, P., Correlation of Reliability Models Including Aging Effects with Thermal Cycling Reliability Data, Electronic Components and Technology Conference, ECTC, 63rd, pp.986-1004, 2013.
5. Lall, P., Shantaram, S., Suhling, J., Locker, D., Effect of Aging on the High Strain Rate Mechanical Properties of SAC105 and SAC305 Lead-free Alloys, Electronic Components and Technology Conference, ECTC, 63rd, pp.1277-1293, 2013.
6. Lall, P., Wei, J., Davis, L., L70 Life Prediction for Solid State Lighting Using Kalman Filter and Extended Kalman Filter Based Models, Electronic Components and Technology Conference, ECTC, 63rd, pp.1452-1465, 2013.
7. Maddox, J., Knight, R., Bhavnani, S., TIM Selection for an IGBT Cold Plate Using Experimental and Numerical Modeling, Proceedings of the ASME InterPACK, InterPACK2013-73207, 2013.
8. Motalab, M., Mustafa, M., Suhling, J., Zhang, J., Evans, J., Bozack, M., Lall, P., Thermal Cycling Reliability Predictions for PBGA Assemblies that Include Aging Effects, Proceedings of the ASME InterPACK, InterPACK2013-73230, 2013.
9. Motalab, M., Basit, M., Suhling, J., Lall, P., A Revised Anand Constitutive Model for Lead-free Solder that Includes Aging Effects, Proceedings of the ASME InterPACK, InterPACK2013-73232, 2013.
10. Hussain, S., Gnanachelvi, P., Suhling, J., Jaeger, M., Hamilton, M., Wilamowski, B., The Influence of Uniaxial Normal Stress on the Performance of Vertical Bipolar Transistors, Proceedings of the ASME InterPACK, InterPACK2013-73233, 2013.
11. Hasnine, M., Mustafa, M., Zou, J., Suhling, J., Prorok, B., Bozack, M., Lall, P., Nanomechanical Characterization of Aging Effects in Solder Joints in Microelectronic Packaging, Proceedings of the ASME InterPACK, InterPACK2013-73234, 2013.
12. Mustafa, M., Roberts, J., Suhling, J., Lall, P., The Effects of Aging of the Cyclic Stress-Strain and Fatigue Behaviors of Lead-free Solders, Proceedings of the ASME InterPACK, InterPACK2013-73240, 2013.
13. Cai, Z., J., Suhling, J., Lall, P., Bozack, M., Aging Induced Mechanical Property Degradation and Microstructure Evolution of SAC+X Lead-free Solder Alloys, Proceedings of the ASME InterPACK, InterPACK2013-73241, 2013.
14. Chhanda, N., Suhling, J., Lall, P., Effects of Moisture Exposure on the Mechanical Behavior of Polymer Encapsulants in Microelectronic Packaging, Proceedings of the ASME InterPACK, InterPACK2013-73242, 2013.
15. Roberts, J., Motalab, M., Hussain, S., Suhling, J., Jaeger, R., Lall, P., Measurement of Microprocessor Die Stress Due to Thermal Cycling, Power Cycling and Second Level Assembly, Proceedings of the ASME InterPACK, InterPACK2013-73244, 2013.
16. Lall, P., Limaye, G., A Methodology for High Cycle Fatigue Characterization of Lead-free Interconnects under Simultaneous Harsh Environments of High Temperature and Vibration, Proceedings of the ASME InterPACK, InterPACK2013-73245, 2013.
17. Lall, P., Limaye, G., Shantaram, S., Suhling, J., Effect of Isothermal Aging and High Strain Rate on Material Properties of Innolot, Proceedings of the ASME InterPACK, InterPACK2013-73246, 2013.
18. Jaeger, R., Motalab, M., Hussain, S., Suhling, J., Four-Wire Bridge Measurements of van der Pauw Stress Sensors on (100) and (111) Silicon, Proceedings of the ASME InterPACK, InterPACK2013-73249, 2013.
19. Lall, P., Sakalaukus, P., Davis, L., Prognostics of Damage Accrual in SSL Luminaires and Drivers Subjected to HTSL Accelerated Aging, Proceedings of the ASME InterPACK, InterPACK2013-73250, 2013.
20. Lall, P., Harsha, M., Suhling, J., Goebel, K., Damage Pre-Cursors Based Prognostication of Accrued Damage and Assessment of Operational Readiness of Lead-free Electronics, Proceedings of the ASME InterPACK, InterPACK2013-73251, 2013.
21. Lall, P., Lowe, R., Goebel, K., Comparison of Prognostic Health Management Algorithms for Assessment of Electronic Interconnect Reliability, Proceedings of the ASME InterPACK, InterPACK2013-73252, 2013.
22. Lall, P., Deshpande, S., Leading Indicators for Prognostics of Impending Failure on Cu-Al Interconnects, Proceedings of the ASME InterPACK, InterPACK2013-73287, 2013.
23. Lall, P., Wei, J., Davis, L., Solid State Lighting Life Prediction Using Extended Kalman Filter, Proceedings of the ASME InterPACK, InterPACK2013-73288, 2013.
24. Lall, P., Zhang, H., Davis, L., Assessment of Lumen Degradation and Remaining Life of LEDs using Particle Filter, Proceedings of the ASME InterPACK, InterPACK2013-73305, 2013.
25. Lall, P., Luo, Y., Resistance Spectroscopy Based Assessment of Degradation in Cu-Al Wire Bond Interconnects, Proceedings of the ASME InterPACK, InterPACK2013-73308, 2013.
26. Lall, P., Mirza, K., Harsha, M., Suhling, J., Method for Assessment of Prolonged and Intermittent Storage on Reliability of Lead-free Electronics using Leading Indicators, Proceedings of the ASME InterPACK, InterPACK2013-73309, 2013.

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